Semester Project

Title: Power supply design procedure
Prepared by: Arion Zimmermann
Reviewed by: Jakub Kucka
Approved by: Prof. Drazen Dujic

Revision History

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1. Abstract

EPFL Xplore's Rover *Argos I* consists of many devices that must be powered at very specific voltages. Using an input voltage ranging from 20V to 30V, the power supply will have to provide six different voltage channels: 3.3V, 5V, 15V, 24V, 48V as well as a bypass channel. The bypass channel can be regarded as an unregulated output that the power supply must monitor. The purpose of the following document is to highlight the different design choices that lead to the conception of a complete power supply. A first working prototype has been developed before starting this semester project. However, since it was designed without any prior power electronics knowledge and the requirements have slightly changed since then, a new design had to emerge. First of all, the new specifications of the power supply will be defined (Section 2) and the decomposition of the supply into subsystems will be performed (Section 3). The following sections of this document will describe the design procedure of every subsystem (Section 4 to 7). Finally, the resulting design will be presented (Section 8).

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2. System specifications

The power supply must accept an input voltage of 20V to 30V. This DC input originates from a battery pack but passes through a circuit breaker and an automotive relay before arriving at the power supply's input.

The supply must be capable of estimating how much charge is left in the battery pack and report it to the teleoperator. This charge estimator must take into account the voltage-charge profile of the battery cells.

Further, an undervoltage protection mechanism must prevent the DC/DC converters from starting switching in an undervoltage condition, which could eventually result in unstable behaviour.

The power supply has to convert its input to different voltage levels. First of all, a 3.3V converter is necessary to power the rover's avionics (embedded sensors). Then, a Raman laser must be powered by a 5V input and 15V must be supplied to the main computer. Further, a LiDAR will have to be supplied with 24V and finally, two ethernet switches require an input voltage of 48V.

Each of these converters must shutdown if their respective connected load exceeds the maximum load they are designed for. Their output power must be measured at any time and reported to the teleoperator. The latter must be able to shutdown any of the converters at any time and expects to receive a "power good" signal from the converter when the output voltage is within 10% of nominal output voltage.

This information must be transmitted to the teleoperator by WiFi directly to the control station in a 2.4GHz band and through the avionics using an I^2C bus.

The input and output connectors of the DC/DC converters must accept cables with diameters ranging from AWG12 and AWG22.

After having identified the power generation and consumption of every device on the Rover, it was possible to define precisely the switching capability of the power supply for every channel. The results are summarised in the tables below.

Input characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Input voltage	Supplied from battery pack	21	25.4	29.4	V
Source impedance	Measured at 1KHz	7	12	16	mΩ
Input current		-	-	25	A

Bypass output characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Output current		-	15	18	A
Output power		-	300	360	W
Nominal load		1.1	1.3	-	Ω
Efficiency	At nominal load	98	-	-	%

3.3V output characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	3	3.3	3.6	V
Output noise & ripple		-	50	100	mVpp
Output current		-	1.12	1.3	A
Output power		-	3.7	4.3	W
Nominal load		2.5	3	-	Ω
Efficiency	At nominal load	80	-	-	%
Efficiency	At half load	70	-	-	%

5V output characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	4.8	5	5.2	V
Output noise & ripple		-	20	50	mVpp
Output current		-	4	5	A
Output power		-	20	25	W
Nominal load		1	1.25	-	Ω
Efficiency	At nominal load	85	-	-	%
Efficiency	At halfload	80	-	-	%

15V output characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	9	15	19	V
Output noise & ripple		-	100	500	mVpp
Output current		-	2.2	3.2	A
Output power		-	33.2	47.5	W
Nominal load		4.7	6.8	-	Ω
Efficiency	At nominal load	90	-	-	%
Efficiency	At half load	85	-	-	%

24V output characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	22	24	26	V
Output noise & ripple		-	100	500	mVpp
Output current		-	0.75	0.85	A
Output power		-	18	22	W
Nominal load		28	32	-	Ω
Efficiency	At nominal load	90	-	-	%
Efficiency	At half load	85	-	-	%

48V output characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	44	48	57	V
Output noise & ripple		-	100	500	mVpp
Output current		-	0.81	0.87	A
Output power		-	39	41.5	W
Nominal load		55	59	-	Ω
Efficiency	At nominal load	90	-	-	%
Efficiency	At half load	85	-	-	%

Measurement characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Battery charge estimator precision	Integrator runs for at most one hour. Expected energy: 600Wh	-	2	5	%
Power measurement precision per channel		-	1	5	%
Power measurement CMRR per channel		80	100	-	dB

RF characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Operating frequency	Central frequency (excluding band channels)	-	2.4	-	GHz
RX sensitivity	Independant from antenna gain	-	-100	-90	dBm
TX power	Independant from antenna gain	18	19	-	dBm
TX signal power		-	-	1	W

Mechanical characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Length	From the battery pack's geometry	165	165	165	mm
Width	From the battery pack's geometry	-	-	120	mm
Height	From the battery pack's geometry	-	20	30	mm
Weight		-	300	400	g
PCB material	Specified by manufacturer (Aisler)	-	FR-4	-	-
Number of PCB layers	Specified by manufacturer (Aisler)	2	4	4	-

Thermal characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
PCB Temperature rise	Tested at full load (all outputs on) at 25°C	-	40	60	K

3. System decomposition

Planning is an important aspect for creating a complex system. It consists of separating the system to design into different independent subsystems, which are then assembled together to form the final system. Those subsystems must implement a set of requirements and a set of interfaces. The purpose of this section is to show the system decomposition and to define the required interfaces. Note that the set of requirements of each subsystem will be developed in other sections.

Hereunder is the system decomposition depicted:

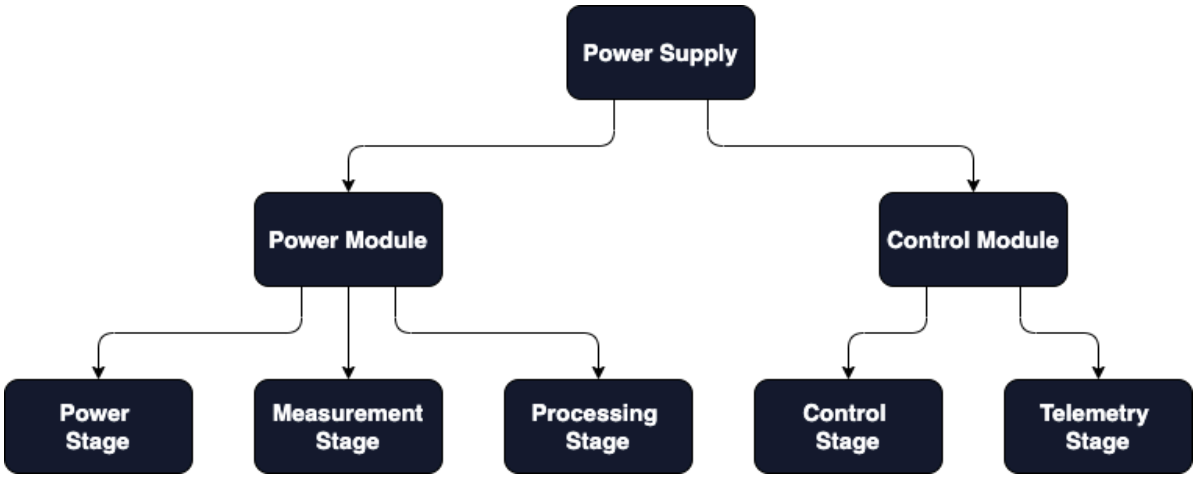


Fig. 2.1: System decomposition into subsystems

The power supply is divided into a power module and a control module. Each of these are further divided into a power stage, a measurement stage, a processing stage, a control stage and a telemetry stage.

The power stage handles the DC/DC conversion of the battery voltage to the desired output channels. The measurement stage reads the output current and voltage of every channel and passes the readings to the processing stage. The latter filters the data and performs computations to estimate the power used by the Rover. The telemetry stage then receives this power consumption measurement and transmits it to the teleoperator. The control stage must also receive this information. If the teleoperator decides to shutdown a specific channel, the telemetry stage receives this order and transmits it to the control stage which directly commands the power stage to shutdown one of its outputs. The control stage is also able to configure the measurement stage. The whole data path is summarised in the graph below:

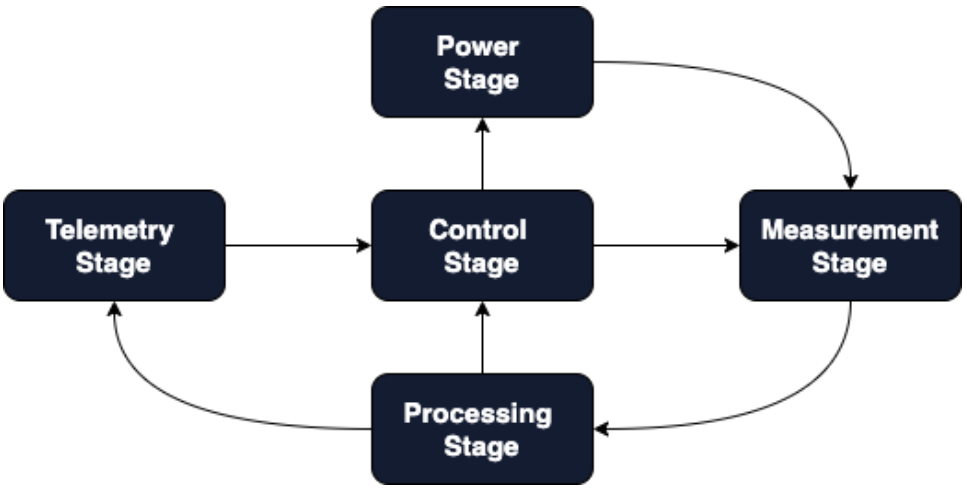


Fig. 2.2: Power supply data path between subsystems

In general, it is preferred to create a physical separation between the subsystems, so that a better modularity can be ensured. However, those physical interfaces may add noise to the shared signals. Therefore, the power module is a monolithic board consisting of the power, measurement and processing stage. Using the same arguments, the control stage and the telemetry stage are on the same physical board.

It is now necessary to define more precisely the different interfaces between the subsystems.

3.1. Interconnect bus interface definition

A physical separation exists between the power module and the control module. This permits to quickly replace the power module or the control module if one of those fails but not the other one. Those two boards are interconnected through a 40-pins connector that allows signals to be transmitted from one board to another. The pin assignment for this connector is very generic to allow forward-compatibility and is described in Appendix A. This bus consists of several subinterfaces: a sensor bus, a control bus, a system bus, a general purpose bus and a status bus.

The schematic corresponding to this interface is shown below for a better understanding.

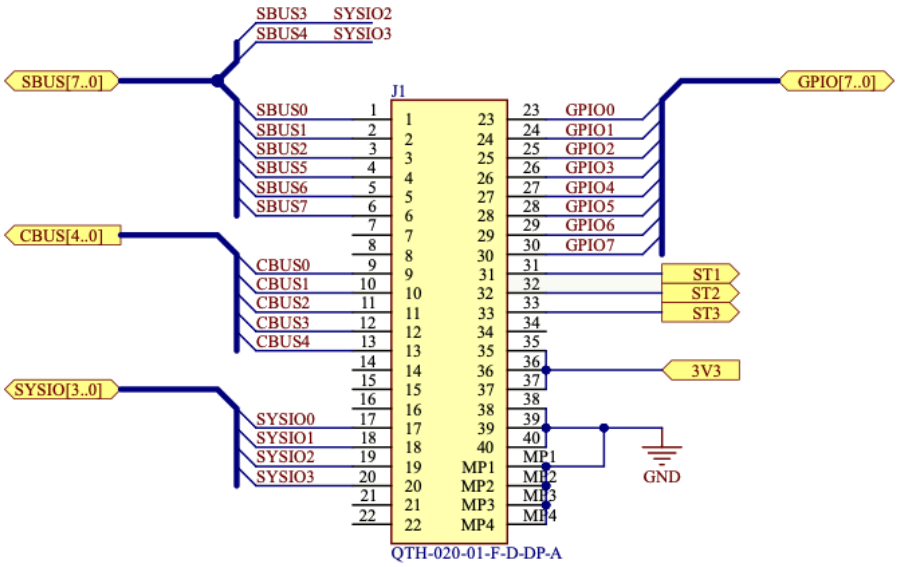


Fig. 2.3: Interconnect schematic (Interconnect.SchDoc)

3.2. Sensor bus interface definition

The link between the control stage and the measurement/processing stage is implemented through the I^2C and SPI protocols. The I^2C is used for low-speed transmission, whereas the SPI is used for high-speed operations. Several address lines are also present in the sensor bus to select which chip must be used in SPI operation. A demultiplexer must transform these address lines into conformal chip-select signals as specified by the SPI protocol. To sum up, this interface can be summarised in the following table.

Pin	Corresponding function
Sensor bus signal 0 (SBUS0)	SPI MISO
Sensor bus signal 1 (SBUS1)	SPI MOSI
Sensor bus signal 2 (SBUS2)	SPI SCK
Sensor bus signal 3 (SBUS3)	I^2C SDA
Sensor bus signal 4 (SBUS4)	I^2C SCL
Sensor bus signal 5 (SBUS5)	SPI address bit 0
Sensor bus signal 6 (SBUS6)	SPI address bit 1
Sensor bus signal 7 (SBUS7)	SPI address bit 2

Table 2.1: Sensor bus interface specification

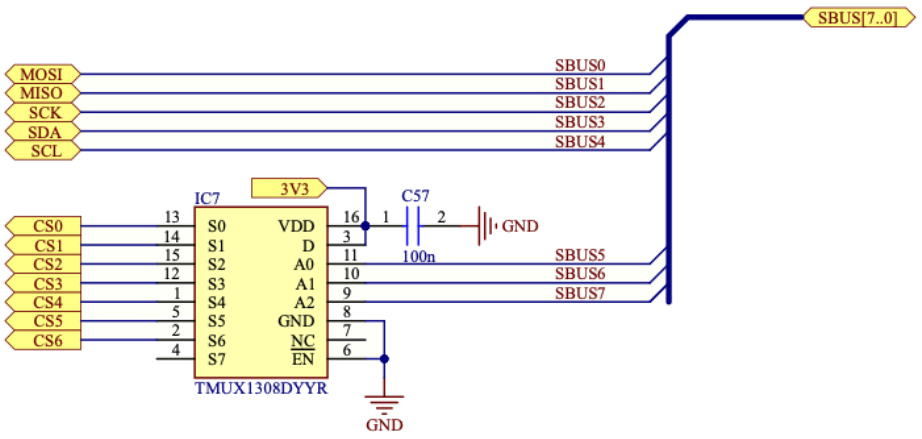


Fig. 2.4: Sensor bus schematic (SensorBus.SchDoc)

The schematic that implements this bus is depicted in Fig. 2.4. The TMUX1308 from Texas Instruments is a simple signal multiplexer/demultiplexer based on transmission gates that converts the SPI address lines into chip-select signals.

3.3. Control bus interface

The control bus allows the control module to start or shutdown a given output channel. To do so, an active low shutdown signal connects the control module to the DC/DC converters. Below is the pin assignment of this interface.

Pin	Corresponding function
Control bus signal 0 (CBUS0)	Shutdown 3.3V output (active low)
Control bus signal 1 (CBUS1)	Shutdown 5V output (active low)
Control bus signal 2 (CBUS2)	Shutdown 15V output (active low)
Control bus signal 3 (CBUS3)	Shutdown 24V output (active low)
Control bus signal 4 (CBUS4)	Shutdown 48V output (active low)

Table 2.2: Control bus interface specification

3.4. System bus interface

This interface is used to connect the power supply to the rest of the Rover. In particular, it consists of an UART link to connect to the Rover's BMS (battery management system) and an I^2C connection to the avionics. Since the I^2C interface is masterless, it has also been connected to the I^2C of the sensor bus interface. Once again, the pin assignments are stated below.

Pin	Corresponding function
System bus signal 0 (SYSIO0)	UART RX
System bus signal 1 (SYSIO1)	UART TX
System bus signal 2 (SYSIO2)	I^2C SDA
System bus signal 3 (SYSIO3)	I^2C SCL

Table 2.3: System bus interface specification

3.5. General purpose bus interface

Eight general purpose lines also connect the control module to the power module. Those are mainly used for debugging purposes. No special protocol is defined for those general purpose signals.

3.6. Status bus interface

To indicate the state of the control module, three signals connect the control module to the power module. These lines shall carry PWM signals whose duty cycle completely defines the state of the control module. Even if the implementation has the right to handle these signals freely, it is clear that this interface is designed to be connected to an RGB LED.

3.7. Power interface

Several ICs must be powered by a 3.3V input. For safety reasons, instead of using the same 3.3V output that powers the Rover's avionics, an auxiliary power supply is added on the power module. All 3.3V sources used in the design are implicitly referring to this auxiliary power supply. The schematics of this power supply is shown in Appendix C.

3.8. Summary

Even though these interface definitions may have been tedious to read, they were necessary for a successful completion of the project. Incomplete interface definitions can cause many problems in later stages of the design process. From there, it is possible to draw a first top-level schematic[1] that can be considered as a block diagram of the system that will be developed in later sections. Please ignore the pull-up resistors for the control lines and the reverse voltage protection diode as the use of those components are very application-specific.

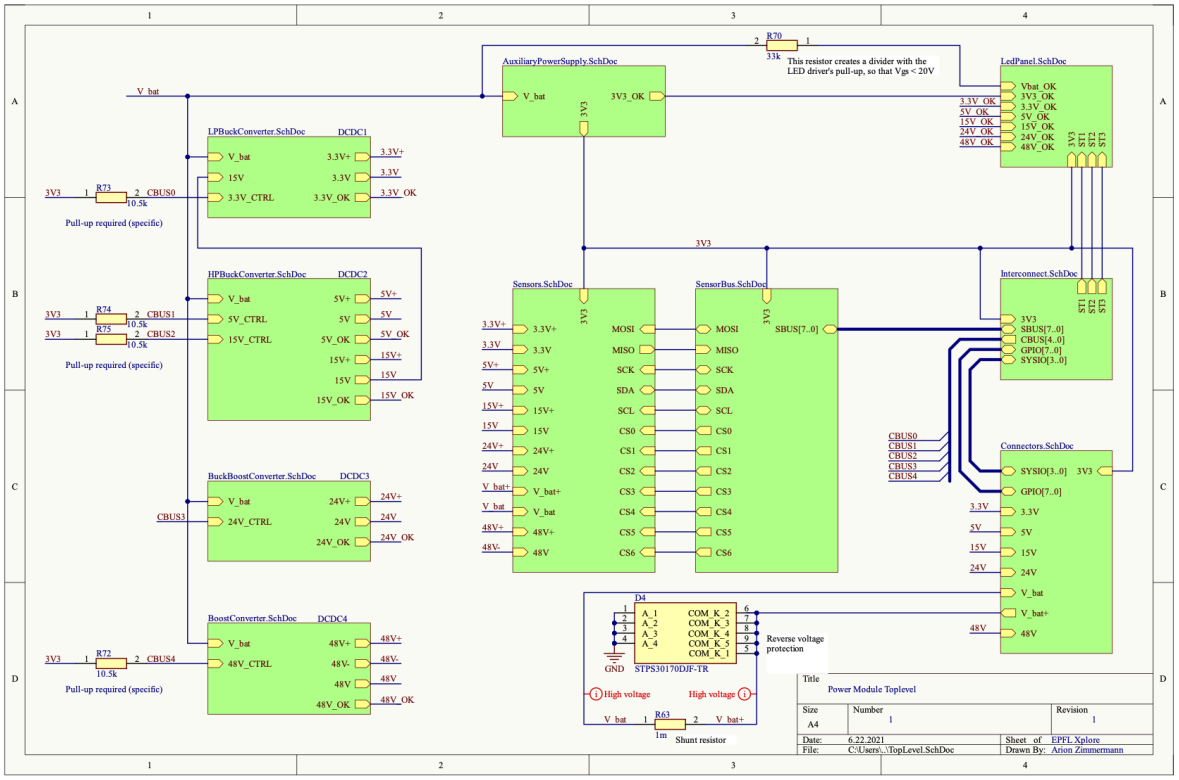


Fig. 2.5: Top-level schematic (TopLevel.SchDoc)

[1] All Altium design files can be found in the folder:
https://drive.google.com/drive/folders/15NjSplxtceq4dqOwnAkcu_aReqRJ0Kdp?usp=sharing

4. Power stage design

4.1. General design considerations

The specifications of the power supply state that 5 different regulated output channels must be provided. However, they do not specify how this is supposed to be achieved and, in particular, which topologies must be used in order to maximise the efficiency and reduce the failure risks.

Let's first create a dependency graph of the different Rover's subsystems and differentiate what is mission critical and what is not. On the one hand, the main computer and the ethernet switches are mission critical and must have their own DC/DC converter to minimise the risk of failure. On the other hand, the avionics, the raman laser and the LiDAR are not mission critical, for the Rover can still operate in certain conditions without these systems.

To maximise the efficiency, it is possible to daisy-chain different DC/DC converters. In table 4.1, all combinations of voltage conversion are listed in order to find the combination that yields the best efficiency. This table is filled with data from the TI Webench tool [RF01] by selecting the desired input/output characteristics and choosing the design that has the best efficiency. Note that it is assumed that the efficiency of those designs will be proportional to an efficiency that could be achieved in the scope of this project.

Input \ Output	3.3V	5V	15V	24V	48V
3.3V	-	95.5%	-	94.8%	-
5V	98.3%	-	-	96.8%	-
15V	96.8%	98.0%	-	98.2%	-
20V - 30V	95.5%	96.9%	98.8%	99.1%	98.6%
24V	95.9%	97.1%	-	-	-
48V	84.8%	96.2%	-	97.9%	-

Table 4.1: Efficiency relations from one voltage to another

Since the overall efficiency of a daisy-chain is the multiplication of the efficiencies of its parts, we can take the logarithm of this table to generate an efficiency graph, and

then apply Dijkstra's shortest path algorithm to find the best daisy-chain combination for each converter, as in Fig. 4.2.

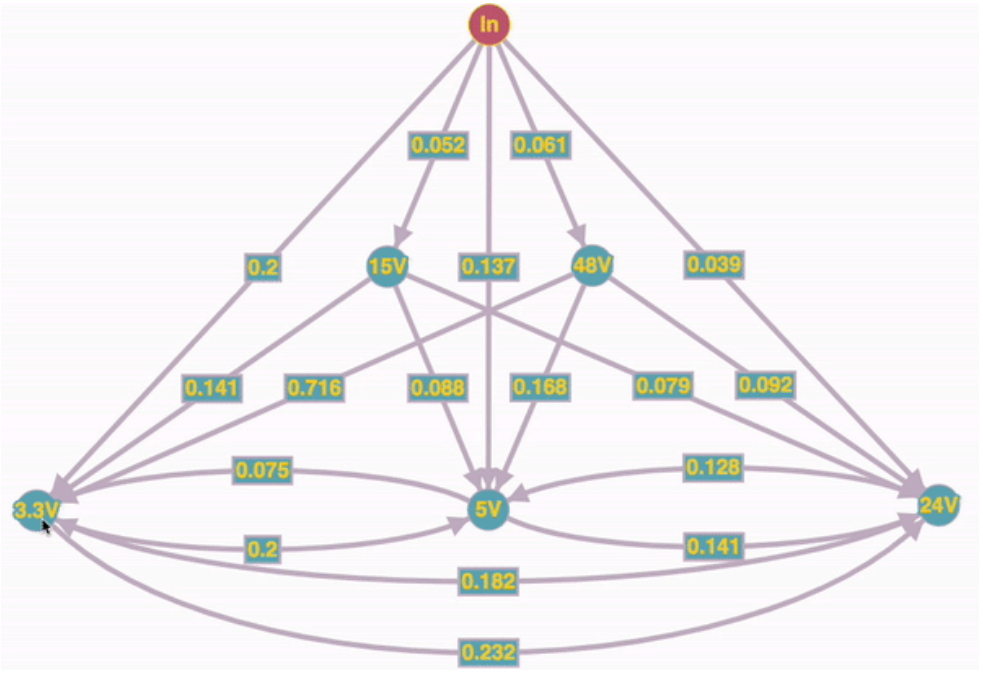


Fig. 4.2: Efficiency graph with weights expressing the attenuation in dB

From this analysis, we conclude that all DC/DC converters will have the battery as their supply, except the 3.3V channel, which will be supplied by the output of the 15V converter. The resulting hierarchy is shown in Fig. 4.3.

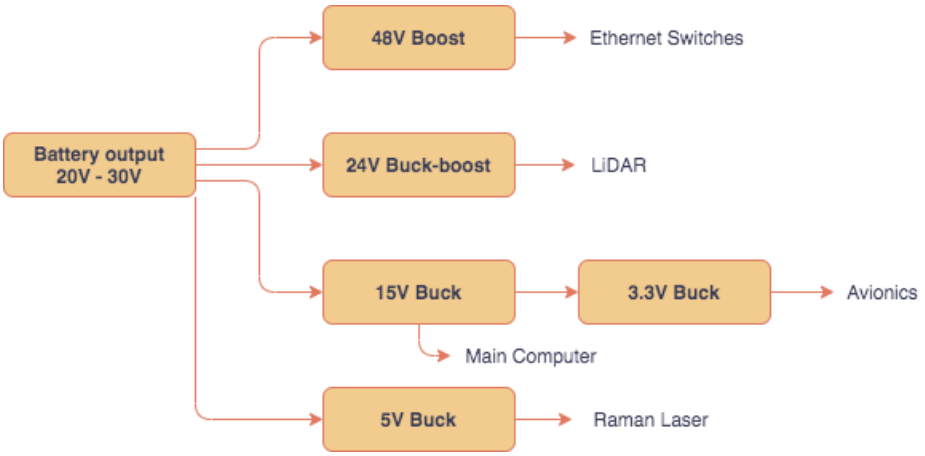


Fig. 4.3: Converters hierarchy. Arrows symbolise the power path.

Let's now consider the different possible topologies for these converters. Since low current passes through these converters, it is not necessary to have galvanic

insulation for the converter stages. It then becomes clear that a boost converter will be used for the 48V output channel and that buck converters are needed for the 3.3V, 5V and 15V converters. The 24V output channel, however, can be implemented in several ways: through the Ćuk, the Buck-boost, the Zeta or the SEPIC topology. The most efficient way, however, to regulate this voltage is to couple a buck and a boost converter and use low on-state resistance MOSFETs. Depending on the input voltage, the controller will enter the buck or the boost topology.

4.2. IC Selection

The selection of the converter IC will be based on multiple criteria that will eliminate unsuitable candidates.
First of all, the input voltage will range from 20V to 30V since the system is powered by Sony Murata VTC6 batteries. Further, to achieve high efficiencies, the converter IC must allow custom frequency selection and synchronous rectification to avoid diode conduction losses. Safety requirements imply input undervoltage protection, current-limiting and soft-start. The ICs shall also have a "power good" feature to provide visual feedback when the IC operates in nominal conditions.
Chips from different manufacturers have been considered in the process: Texas Instruments, Analog Devices, Microchip, ON semiconductors, STMicroelectronics and Maxim integrated.
Since more than a single IC matching the given constraints will likely be found, let's also take note of the estimated efficiency given in the datasheet at nominal load and the minimal achievable switching frequency. It is true that these metrics alone do not provide meaningfully comparable values, especially since the testing conditions differ from one chip to another and from one manufacturer to another. Together though, these metrics give a good performance overview.
It is therefore considered that a chip is more performant than another if its efficiency is greater and its minimal switching frequency lower.

4.2.1. Buck converters selection

From the general design considerations, it was possible to conclude that a first stage of buck converters was needed to reach the 15V and 5V output levels. In order to reduce the complexity of the system, a single 2-channels converter IC is preferred to reach the 5V and 15V. As a reminder, the following tables give the output specifications for the 5V and the 15V channel.

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	4.8	5	5.2	V
Output current		-	4	5	A
Output power		-	20	25	W

Table 4.1: 5V output characteristics summary

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	9	15	19	V
Output current		-	2.2	3.2	A
Output power		-	33.2	47.5	W

Table 4.2: 15V output characteristics summary

Looking at every part available from every manufacturer specified above, the following chips matching the requirements could be found.

Manufacturer	Part number	Min. freq.	Price (CHF)	Availability
Analog Devices	LTC3892	75kHz	10.45	400
Analog Devices	LTC3802	330kHz	10.16	40
Maxim Integrated	MAX17558	350kHz	5.40	400

Table 4.3: Candidate ICs for the dual buck converter

From this table, the LTC3892 [RF02] was selected to power the raman laser and the main computer since it can achieve very low frequencies.

Furthermore, the 3.3V channel powering the Avionics will be supplied directly from the output of the 15V channel.

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	3	3.3	3.6	V
Output current		-	1.12	1.3	A
Output power		-	3.7	4.3	W

Table 4.4: 3.3V output characteristics summary

Once again, looking at every part available in the market matching the specifications, the following table that summarises their characteristics could be created.

Manufacturer	Part number	Est. efficiency	Min. freq.	Price	Availability
Analog devices	LT8609	90%	200kHz	6.06	2500
Analog devices	LTC3126	93%	200kHz	8.36	1100
ON semiconductor	FAN2103	86%	200kHz	4.55	2000

Table 4.5: Candidate ICs for the 3.3V channel

Even though it is expensive, the LTC3126 [RF03] seems to be a superior chip in terms of estimated efficiency and of minimum switching frequency. This is the chosen chip to convert 15V to 3.3V.

Now that each and every buck converter of the system has been selected, the buck-boost converter must be considered.

4.2.2. Buck-boost converter selection

The LiDAR's 24V power supply must fit the following constraints.

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	22	24	26	V
Output current		-	0.75	0.85	A
Output power		-	18	22	W

Table 4.6: 24V output characteristics summary

These constraints, along with the general requirements reduced the IC selection process significantly. In fact, only one chip standed out for these specifications.

Manufacturer	Part number	Est. efficiency	Min. freq.	Price	Availability

Texas Instruments	LM5175	95%	100kHz	5.78	1000

Table 4.7: Candidate ICs for the 24V channel

The LM5175 [RF04] will be utilised to power the Rover's LiDAR. Finally, only the boost converter remains to be selected.

4.2.3. Boost converter selection

A 48V DC-DC converter is needed to power the ethernet switches. The supply will be powered directly by the batteries having a voltage ranging from 20V to 30V. The following table displays the constraints defined by the power budget that the supply must comply with.

Parameter	Comment	Min.	Typ.	Max.	Unit
Output voltage	At nominal load	44	48	57	V
Output current		-	0.81	0.87	A
Output power		-	39	41.5	W

Table 4.8: 48V output characteristics summary

On the basis of these constraints, a few ICs available on the market could be isolated on the table below.

Manufacturer	Part number	Min. freq.	Price	Availability
Analog devices	LTC7871	60kHz	7.62	300
Analog devices	LT8228	80kHz	14.21	300
Maxim Integrated	MAX17498B	250kHz	2.15	2000

Table 4.9: Candidate ICs for the 48V channel

Quick comparison of the models shows that the MAX17498B might not be the best-suited chip for this project since its minimum switching frequency is relatively

high. Comparing the datasheets of LTC7871 and LT8228 in detail, one finds that the LT8228 is less complex and can achieve better performance in low load conditions. Since this 48V channel is supposed to power cameras, those might not be enabled during the whole mission, and the Rover might demand less power from the 48V channel. This is why the LT8228 [RF05] is chosen to power the PoE (Power over Ethernet) switches.

4.2.4. Summary

To sum up this section, the following BOM lists the different converter ICs that will be used for the power supply.

Channel	Part number	Price	Weight	Availability
3.3V	LTC3126	CHF8.36	0.25g	1100
5V / 15V	LTC3892	CHF10.45	0.42g	400
24V	LM5175	CHF5.78	0.07g	1000
48V	LT8228	CHF14.21	3.6g	300

Table 4.10: Selected ICs bill of materials

4.3. MOSFET Selection

Choosing the right MOSFET depends on a lot of factors. In order to get comparable results throughout the selection process, the switching frequency is fixed at 100kHz and the input voltage is kept at 25V. The losses across a MOSFET are due to two phenomena: the conduction losses because of the ON-resistance of the transistor and the switching losses due the charge accumulated on the semiconductor junctions.

On the one hand, the conduction losses are relatively easy to compute:

$$P_{cond,MOSFET} = R_{DS(on)} * I^2_{MOSFET,RMS}$$

On the other hand, the switching losses have many dependencies on the MOSFET characteristics. First, the voltage rise and fall times on the gate must be computed. Then, the energy stored on the junctions of the transistor has to be considered, which finally leads to the computation of the switching losses.

$$tru_{1,2} = (U_{DD} - R_{Ds(on)} * I_{Don}) * R_G \frac{C_{GD1,2}}{U_{plateau}}$$

$$tfu_{1,2} = (U_{DD} - R_{Ds(on)} * I_{Don}) * R_G \frac{C_{GD1,2}}{U_{Dr} - U_{plateau}}$$

$$tru = \frac{tru_1 + tru_2}{2}$$

$$tfu = \frac{tfu_1 + tfu_2}{2}$$

$$E_{on,M} = U_{DD} * I_{Don} * \frac{tri + tfu}{2} + Q_{rr} * U_{DD}$$

$$E_{off,M} = U_{DD} * I_{Doff} * \frac{tru + tfi}{2}$$

$$P_{on,off,MOSFET} = E_{on,off,M} * f_s$$

U_{DD} is the supply voltage, $R_{DS(on)}$ is the ON resistance at the operating conditions, I_{Don} is the ON-state current of the MOSFET, R_g is the gate resistance, $U_{plateau}$ is the Miller plateau voltage, U_{DR} is the gate drive voltage, Q_{RR} is the reverse recovery charge, tri/tfi are the current rise and fall times at nominal current, and $C_{GD}(V)$ is the gate-drain junction capacitance with respect to the drain-source voltage . Further, C_{GD1} is C_{GD} evaluated at U_{DD} and C_{GD2} is C_{GD} evaluated at $R_{DS(on)}$ I_{on}. These equations come from [RF06] (Infineon, D. Graovac). From these relations, an excel spreadsheet [RF07] was created to quickly estimate the power dissipation of a MOSFET. The breakdown voltage of these transistors must be at least 200% of the maximum input voltage to

overcome voltage transients, ie. 60V. The same safety margin applies to the continuous drain current, which must be 150% of the maximum nominal current. To reduce the switching loop area and thus the EMI, let's first select 2-channels MOSFETs for every synchronous pair. The MOSFETs must be RoHS compliant. These requirements reduce the choice to 35 different MOSFETs which have an on-state resistance less than 50mΩ on Mouser.

For each of these MOSFETs, their main characteristics were extracted from the datasheet and entered on the spreadsheet to facilitate the computation of losses [RF07]. To select a MOSFET, only several converter characteristics must be entered on the spreadsheet, such as the high-side voltage, the duty cycle, the drain current, the drain current ripple and the switching frequency. The spreadsheet then computes the losses generated by each of the 35 MOSFETs and we pick the one with least losses. It is also important to filter the resulting MOSFETs by their drain-source safe operating area: the transistors must withstand 24V DC voltage at the rated current, taking temperature derating into consideration.

On the table below, the resulting MOSFETs were selected according to their respective channels. Note that the 3.3V converter has integrated transistors.

Searching on Mouser for different MOSFETS satisfying the requirements and sorting them by on-state resistance yields the following table for the 5V channel.

Channel	Manufacturer	Model number	Resistance	Computed losses
5V	Diodes incorporated	DMTH6016LSDQ	14mΩ	152mW
15V	Diodes incorporated	DMTH6016LSDQ	14mΩ	141mW
24V buck	ON semiconductor	NVMFD5C680NLWFT1G	20mΩ	39mW
24V boost	Diodes incorporated	DMTH6016LSDQ	14mΩ	35mW
48V	ON semiconductor	NVMFD5C680NLWFT1G	20mΩ	50mW

Table 4.11: Candidate dual-channel MOSFETs

Let's now consider another design, using single channel MOSFETs. To compete with the dual channel switches, it is necessary for the transistor's footprint to be small, at least thrice as small as the selected dual channel MOSFETs. The only MOSFET series satisfying this requirement is the BSZ 60V OptiMOS 5 line from Infineon Technologies, with a footprint smaller than 10mm^2. The following table depicts the losses for every channel.

Channel	Manufacturer	Model number	Resistance	Computed losses
5V	Infineon Technologies	BSZ0703LS	5.4mΩ	64mW
15V	Infineon Technologies	BSZ0703LS	5.4mΩ	62mW
24V buck	Infineon Technologies	BSZ099N06LS5	8mΩ	22mW
24V boost	Infineon Technologies	BSZ099N06LS5	8mΩ	18mW
48V	Infineon Technologies	BSZ099N06LS5	8mΩ	15.9mW

Table 4.12: Candidate single-channel MOSFETs

To simplify the BOM and still have a highly efficient design, BSZ099N06LS5 [RF08] MOSFETs will be used for the next steps of this project.

4.4. Passive components selection

Let's set some constraints for the passive components. First, every IC in the circuit is allowed to have an inductor current ripple of 30% of their respective average inductor current. Further, a primary input capacitor should withstand 1ms faults and a secondary ceramic input capacitor should provide energy to the converter's hot loop. For the first bulk capacitor, its energy divided by the 1ms fault time should be enough to maintain a rated voltage (20V), assuming a nominal voltage when the fault occured (24V).

$$E = \frac{1}{2}C(V_2^2 - V_1^2) = \frac{P_{out}}{f_{sw}}$$
$$C_{in} = \frac{2P_{out} * 1ms}{176V^2} = 5.68 * P_{out}\frac{\mu F}{W}$$

The secondary capacitor must maintain an almost constant voltage throughout the switching periods. During one period, the system converts energy from the capacitor to the output. Allowing a 15% voltage drop across the capacitor and solving for C yields:

$$C_{in,x} = \frac{2P_{out}}{f_{sw} * 160V^2}$$

Setting the switching frequency to 100kHz, one obtains

$$C_{in,x} = P_{out} * 125nF/W$$

Polymer Tantalum capacitors will be chosen for the bulk capacitors (input and output capacitors) since they have very low ESR and no DC bias derating.

4.4.1. 3V output channel

The 3.3V buck converter can have its frequency as low as 200kHz. Since this channel will generate 1.3A at 3.3V, the inductor average current is also 1.3A and is sourced by a 15V input voltage. The output voltage ripple must be limited to 100mVpp of the nominal output voltage. From these considerations, the following relations hold:

$$L_{min} = \frac{1}{f\Delta I_L}V_{out}(1 - \frac{V_{out}}{V_{in}}) = 33\mu H$$

Chosen part: **Coilcraft SER2211-473MED** (47µH, 10.7mΩ, 14g)

$$C_{out,min} = \frac{\Delta I_L}{8 f \Delta V_{out}} = 2.4\mu F$$

For better loop stability, a higher value capacitor with lower ESR is preferred.
Chosen part: **KEMET T521X476M035ATE030** (47µF, 30mΩ)

Since the 3.3V channel is sourced from the 15V channel, particular attention must be given to the input capacitor. In fact, the 15V channel not only provides power to the 3.3V converter, but also to the main computer. This main computer may draw transient currents from the supply, which enforces the implementation of a stronger fault-immunity for the 3.3V channel. Let's assume that these current transients last for less than 5ms. The bulk input capacitor expression becomes:

$$C_{in} = P_{out} * 28.4 \frac{\mu F}{W} = 122\mu F$$

Chosen part: **KEMET T523H107M035APE070** + **T598D336M035ATE065** (133µF)

4.4.2. 5V output channel

The dual buck converter can achieve a switching frequency as low as 75kHz. To get a documented behaviour, a switching frequency of 105kHz was chosen and the passive components were selected with respect to this value. Since this channel will generate 5A at 5V, the inductor average current is also 5A. The output voltage ripple must be limited to 50mVpp of the nominal output voltage. Note that the input capacitance will be computed for the 15V channel only since the dual converters operate out-of-phase. From these considerations, the following relations hold:

$$L_{min} = \frac{1}{f \Delta I_L} V_{out} (1 - \frac{V_{out}}{V_{in}}) = 33\mu H$$

Chosen part: **Wurth Elektronik** 74436413300 (33µH, 1.6mΩ, 38g)

$$C_{out,min} = \frac{\Delta I_L}{8 f \Delta V_{out}} = 2.4\mu F$$

Chosen part: **KEMET T521X476M035ATE030** (47µF, 30mΩ)

$$C_{in,x} = P_{out} * 125 \frac{nF}{W} = 3.1\mu F$$

Chosen part: **AVX 22201C106KAT2A** (10µF)

4.4.3. 15V output channel

For the 15V channel, the same switching frequency assumption can be made as for the 5V channel. The switching frequency is thus set at 105kHz. This channel has a maximum output current of 3.2A and 500mVpp maximum output voltage ripple. Expressions for L_{min} and $C_{out,min}$ are:

$$L_{min} = \frac{1}{f\Delta I_L} V_{out}(1 - \frac{V_{out}}{V_{in}}) = 33\mu H$$

Chosen part: **Wurth Elektronik 74437529203680** (68µH, 11.33mΩ, 35g)

$$C_{out,min} = \frac{\Delta I_L}{8f\Delta V_{out}} = 2.4\mu F$$

Chosen part: **KEMET T521D475M063ATE075** (4.7µF, 75mΩ)

Moreover, the sourcing of the converter's hotloop is managed by a ceramic capacitor.

$$C_{in,x} = P_{out} * 125\frac{nF}{W} = 6F$$

Chosen part: **AVX 22201C106KAT2A** (10µF)

Since the dual channel converter operates in a 180° phase shift between the channels, a DC current flows from the main supply to the converters. In theory, this means that there is no need for a bulk input capacitor. Nonetheless, it is assumed that this out-of-phase operation might not be perfect and that 0.1ms transients could be drawn from the bulk input capacitor for the LTC3892.

In equations,

$$C_{in} = \frac{2P_{out} * 1ms}{176V^2} = 1.14 * P_{out}\frac{\mu F}{W} = 54.7\mu F$$

Chosen part: **Kemet T521X476M035ATE030** + **Kemet T598D336M035ATE065** (80µF, <65mΩ)

4.4.4. 24V output channel

The capacitors and inductors for the 24V channel are defined by the channel's specifications: Max. current of 0.85A and max. output voltage ripple of 500mVpp. Due to the way the LM5175 IC operates, the inductor must be designed to

match the 30% limit for both the buck and the boost operating modes. To find a suitable inductor, it is necessary to consider the buck as well as the boost mode. A switching frequency of 110kHz was chosen.

$$L_{min,buck} = \frac{1}{f\Delta I_L} V_{out}(1 - \frac{V_{out}}{V_{in}}) = 171\mu H$$

$$L_{min,boost} = \frac{1}{f\Delta I_L} \frac{V_{in}^2}{V_{out}}(1 - \frac{V_{in}}{V_{out}}) = 99\mu H$$

Chosen part: **Wurth Elektronik 74437529203221** (220µH, 36.5mΩ, 35.2g)

Since the topology of the converter is the daisy chain of a buck and a boost converter, it is necessary to provide two input and two output capacitors. In the buck operation, the input capacitor provides power to the hotloop, thus requiring an input ceramic capacitor. In contrast, the boost operation requires an output ceramic capacitor to source the converter's switching loop. The value of the capacitor is however calculated in the same way as with the input ceramic capacitor in buck topology.

$$C_{out,min} = \frac{\Delta I_L}{8f\Delta V_{out}} = 2.4\mu F$$

For better loop stability, a higher value capacitor with lower ESR is preferred.
Chosen part: **KEMET T521X476M035ATE030** (47µF, 30mΩ)

$$C_{in} = 6.25 * P_{out}\frac{\mu F}{W} = 138\mu F$$

Chosen part: **Kemet T523H107M035APE070** + **T521X476M035ATE030** (147µF, 65mΩ)

$$C_{in,x} = C_{out,x} = P_{out} * 125\frac{nF}{W} = 3.0F$$

Chosen part: **AVX 22201C106KAT2A** (10µF)

4.4.5. 48V output channel

Finally, the 48V channel admits a 1Vpp output voltage ripple and can achieve a switching frequency as low as 80kHz. Nonetheless, to reduce the weight of the power supply and limit the inductor's DCR, a higher switching frequency of around 160kHz was selected. Moreover, since the output voltage ripple requirement can be

easily achieved, let's rather set it to 100mVpp. The converter's inductors and capacitors are found in the following manner:

$$L_{min} = \frac{1}{f\Delta I_L}\frac{V_{in}^2}{V_{out}}(1 - \frac{V_{in}}{V_{out}}) = 168\mu H$$

Chosen part: **Wurth Elektronik 74437529203221** (220µH, 36.5mΩ, 35.2g)

$$C_{out,min} = \frac{\Delta I_L}{8f\Delta V_{out}} = 2.4\mu F$$

Chosen part: **Kemet T521D475M063ATE075** (4.7µF, 75mΩ)

The output capacitors feel a 48V potential difference between their terminals. The output ceramic capacitor is allowed to drop only 15% of its voltage during a switching cycle.

In equations,

$$E = \frac{1}{2}C^2 * 48^2V^2 * (1 - 0.85^2) = \frac{1}{2}C^2 * 639V^2$$

Solving for C yields:

$$C_{out,x} = \frac{2P_{out}}{f_{sw} * 639V^2} = 3.6\mu F = 901nF$$

Chosen part: **TDK C3216X8L1H155K160AC** (1.5uF)

Finally, the bulk input capacitor is calculated as before:

$$C_{in} = 6.25 * P_{out}\frac{\mu F}{W} = 138\mu F$$

Chosen part: 3x **Kemet T523H107M035APE070** (100µF, 70mΩ)

4.4.6. Summary

The selected passive components were compiled in the following two bills of materials to have a quick reference.

Part number	Count	Value	DCR	Saturation current	Weight	Subtotal
74436413300	1	33µH	1.31mΩ	6A	37.79g	CHF7.60
SER2211-473MED	1	47µH	8.95mΩ	4.4A	13.5g	CHF5.44
74437529203680	1	68µH	10.3mΩ	10.6A	35.22g	CHF8.58
74437529203221	2	220µH	36.45mΩ	5.3A	35.18g	CHF8.58

Table 4.13: Inductors bill of materials

Part number	Count	Value	ESR	Voltage	Weight	Subtotal
T521D475M063ATE075	3	4.7µF	75mΩ	63V	1.2g	CHF15.27
T598D336M035ATE065	2	33µF	65mΩ	35V	0.4g	CHF5.10
T521X476M035ATE030	4	47µF	30mΩ	35V	1.8g	CHF18.24
T523H107M035APE070	5	100µF	70mΩ	35V	4.15g	CHF28.25

Table 4.14: Polymer Tantalum electrolytic capacitors bill of materials

4.5. Schematics

Now that the most critical components have been selected, the schematics for the DC/DC converters can be drawn. Note that little details are given in this section since most of the schematics design consists of applying equations given in the datasheet of the converters.

4.5.1. 3V buck converter

The LTC3126 buck converter is used to provide a 3.3V output channel. This IC features integrated MOSFETs, which makes it the simplest DC converter in the power module. As discussed in section 4.1, it is more efficient to power this converter from the 15V output channel. Nonetheless, to reduce the risk of failure, this chip can accept two supply voltages. If the 15V output channel is not outputting the correct voltage, the LTC3126 will fallback to the battery voltage.

For this design, the undervoltage condition for a 15V input is set to occur when this input voltage drops to 10V. Similarly, the battery input is considered as invalid when its voltage drops below 18V. This IC is designed to operate at 200kHz. Note that the feedback compensation capacitor equation was computed using a datasheet's formula.

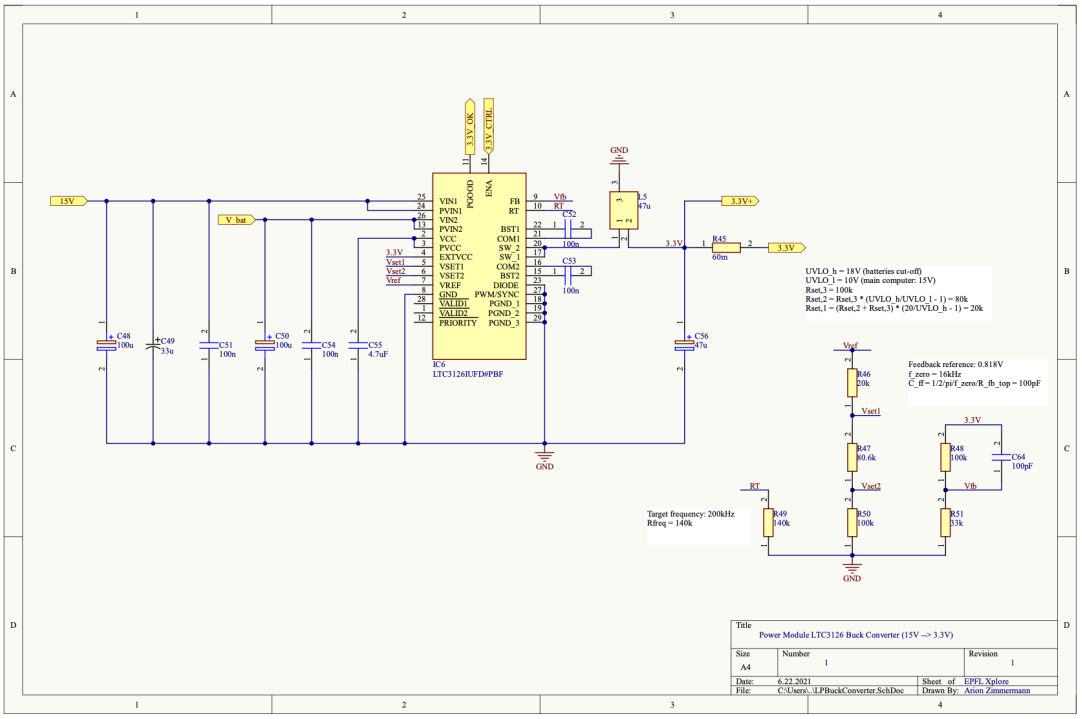
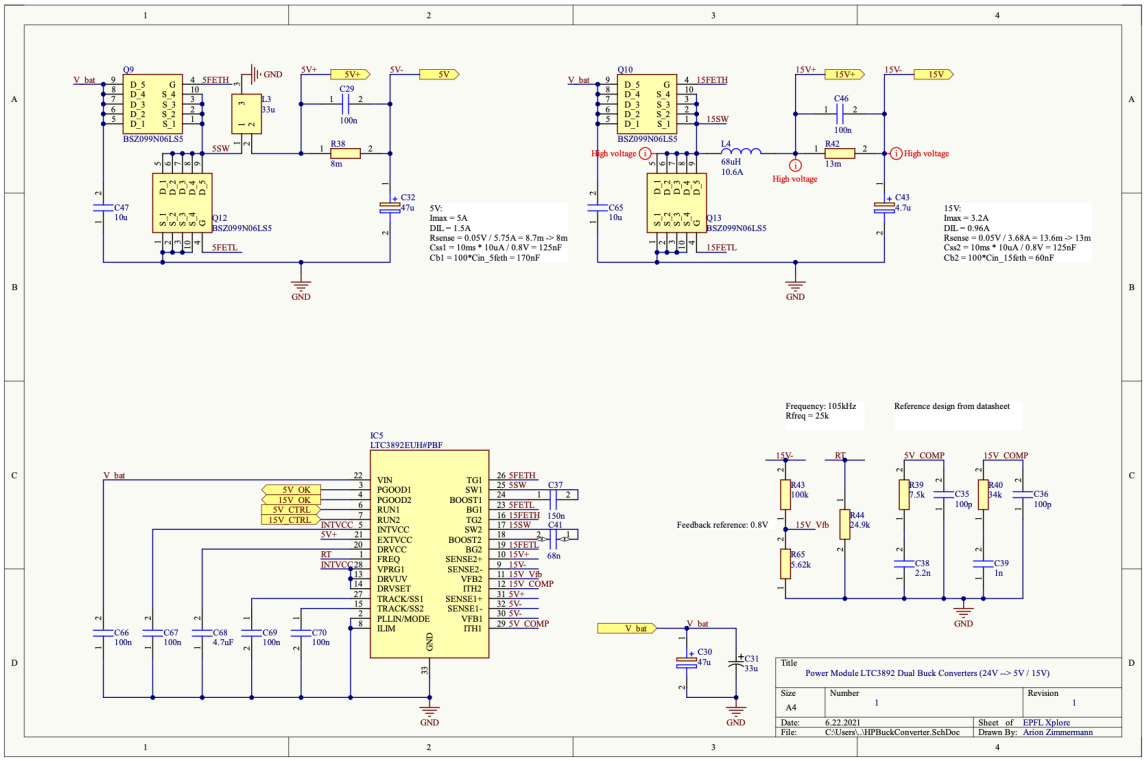


Fig. 4.4: 3.3V buck converter schematic (LPBuckConverter.SchDoc)

4.5.2. 5V / 15V buck converter

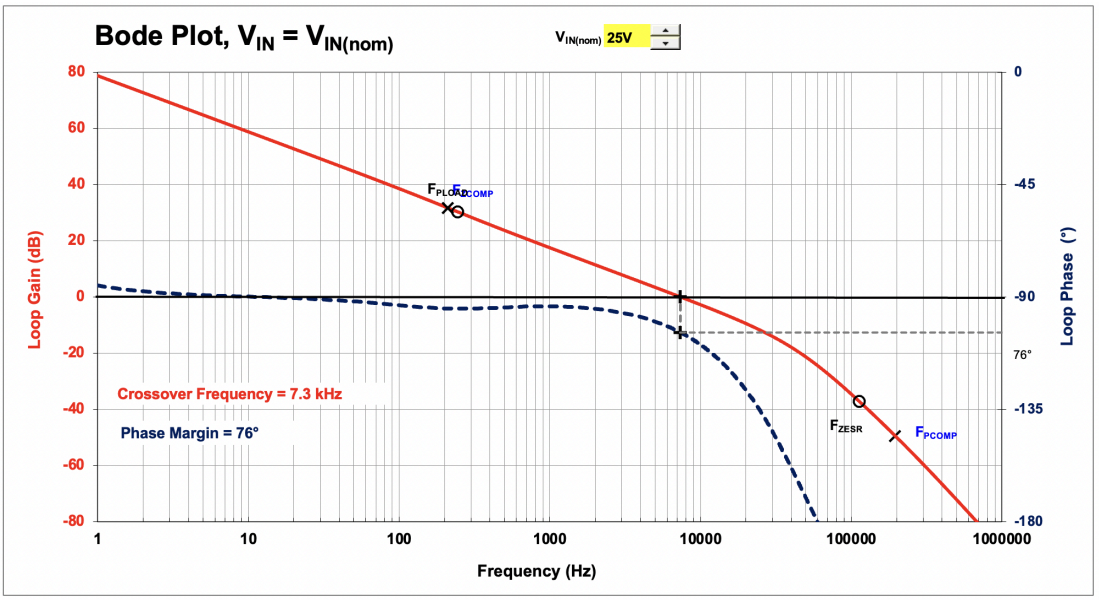
The dual-channel buck converter that outputs 5V and 15V is slightly more complex than the 3.3V converter. In fact, in-rush current control, current limit, gate drive voltage and compensation networks can be programmed. To limit in-rush current, the soft-start capacitor is designed to charge itself in 10ms. The current limit is set to 6.25A and 3.8A for the 5V and the 15V respectively and the MOSFET driving voltage is set to 10V. Moreover, the compensation networks are set according to the datasheet's reference design because its specifications are very similar to the ones I'm implementing. Finally, the switching frequency of this converter is set to 105kHz.



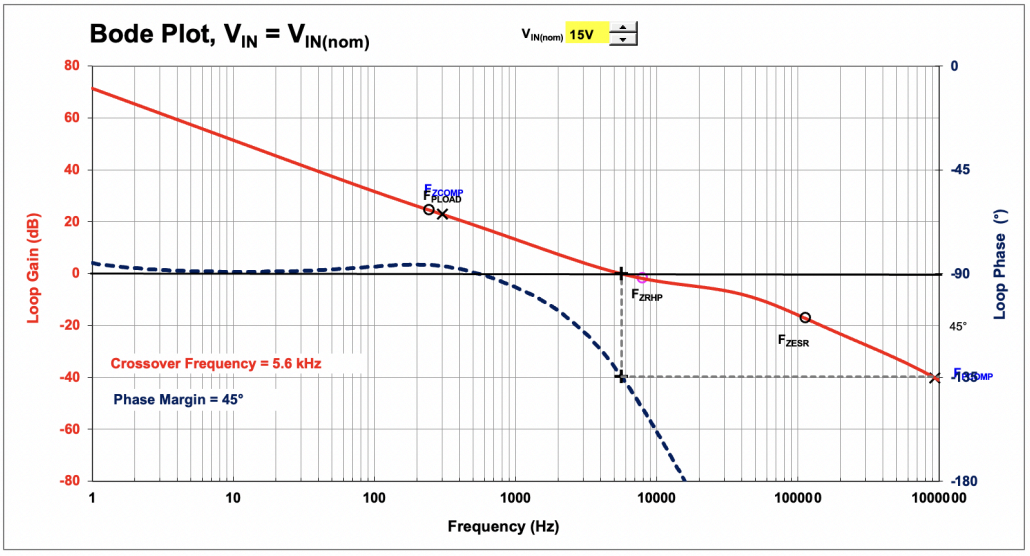
4.5.3. Fig. 4.5: 5V/15V dual-buck converter schematic (HPBuckConverter.SchDoc)

4.5.3. 24V buck-boost converter

The LM5175 buck-boost converter is even more complex than the dual-channel buck converter. The chip provides the regulated output voltage through a full-bridge configuration and therefore requires four MOSFETs. It also requires bootstrap supplies for the gate drivers and special filtering for current limiting. Soft-start is set to last for 10ms and the IC enters an undervoltage condition when the input voltage falls below 15V. For the LM5175, a compensation network design tool is provided [RF09]. A good frequency response should be attained by setting the cross-over frequency to around 8kHz. The bode plot of the whole system is shown below in different operating conditions. The phase margin is always greater than 45°.



4.5.5. Fig. 4.6: Bode plot of the converter's frequency response at nominal input



4.5.6. Fig. 4.7: Bode plot of the converter's frequency response at worst-case input

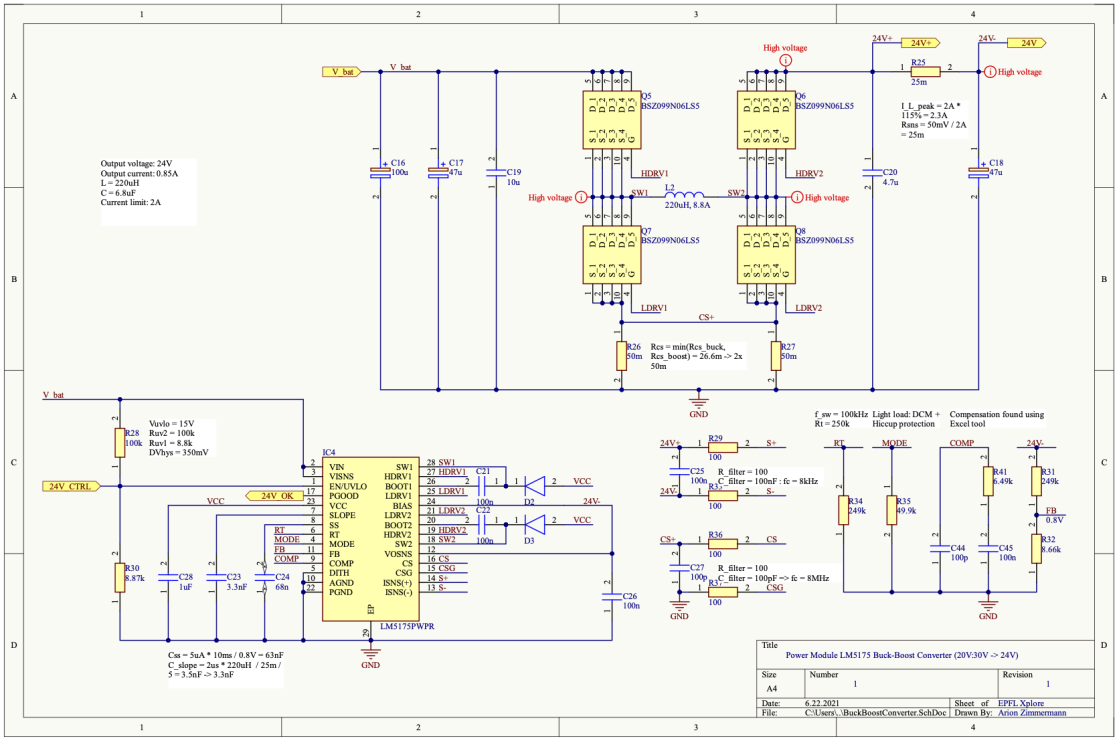


Fig. 4.8: 24V buck-boost converter schematic (BuckBoostConverter.SchDoc)

4.5.4. 48V boost converter

The boost converter is by far the most complex DC/DC converter on the power module, for this IC allows bidirectional power conversion. Not only can it handle 24V to 48V conversion, but it can also handle 48V to 24V. The advantage of such a chip is the ability to change from a 24V battery pack to a 48V battery pack, when necessary. External MOSFETs allow immediate shutdown of input or output when there is a fault. Current limiting is handled on the input and the output stage and two independent feedback loops handle the 24V and the 48V stages. The compensation networks advised by the datasheet were used for this design.

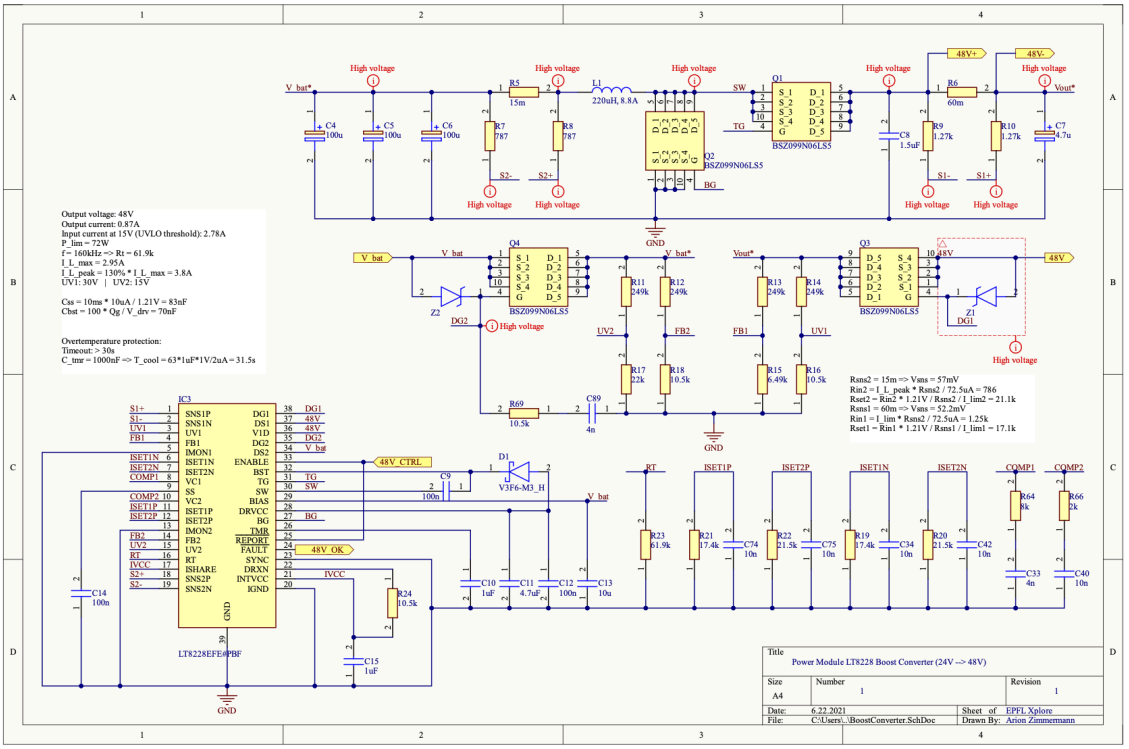


Fig. 4.9: 48V boost converter schematic (BoostConverter.SchDoc)

4.6. PCB Layout

The power module is designed as a four-layers PCB. The different layers were named from top to bottom in the following manner:

- PL1: Power Layer 1
- PL2: Power Layer 2
- SL1: Signal Layer 1
- SL2: Signal Layer 2

The logic of this layer stack-up is to isolate as much as possible the sensitive lines from the noisy lines. Typically, the PL1 contains most of the power planes, as well as the switching loops, whereas the SL2 is mainly used by sensitive analog signal lines that are used for power measurements.

The PCB design itself was focused on several key aspects:

- Minimising EMI
- Maximising heat dissipation
- Minimising differential noise on analog lines

To minimise EMI, it is necessary to reduce the area of the switching loop as much as possible. For the buck topology, this switching area consists of the bypass input ceramic capacitor and the two MOSFETs. For the boost topology, this area consists of the two MOSFETs and the bypass output capacitor.

For better heat dissipation, large copper areas were created around the MOSFETs and the converter ICs. Thermal vias were also placed to facilitate natural convection.

Current sensing lines were often necessary to limit the current of buck converters. To minimise the sensing errors, the differential lines were tightly packed together, so that only common-mode noise would be picked up by the signal. Furthermore, kelvin connections were made between the current sense resistor and the differential signal. In addition, large ground planes were placed on the four layers. Finally, particular care was taken to make those ground planes as little inductive as possible by placing bypass vias when the plane was cut by a signal.

To show the design style that was adopted, the PCB layout for the 48V output is displayed and annotated below as an example.

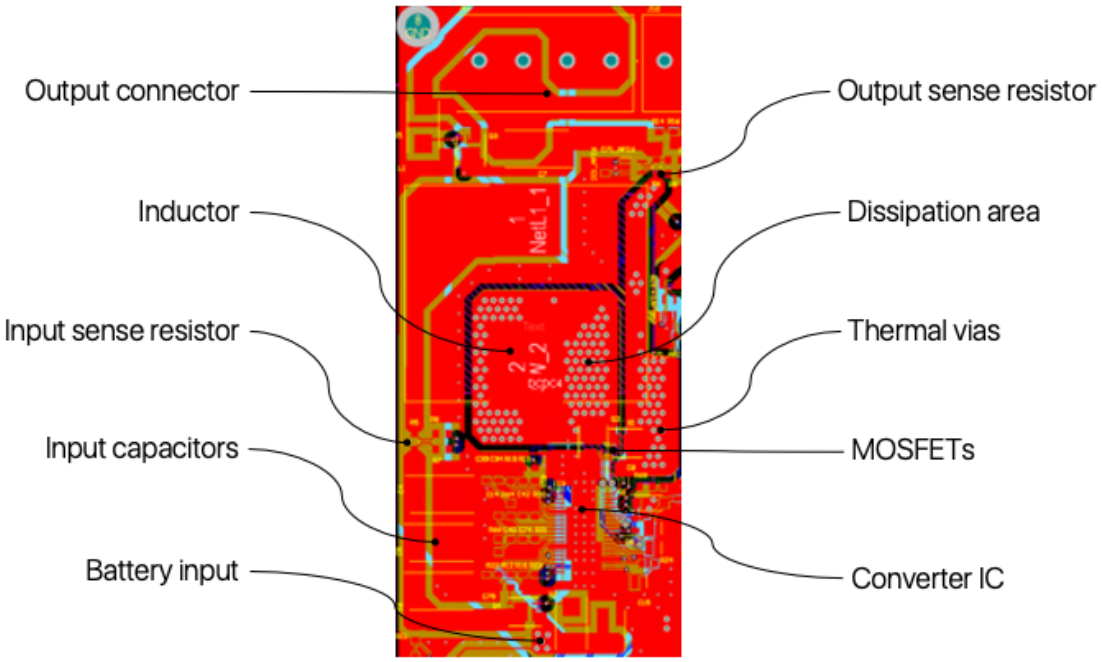


Fig. 4.10: 48 boost converter PCB layout (PowerModule.PcbDoc)

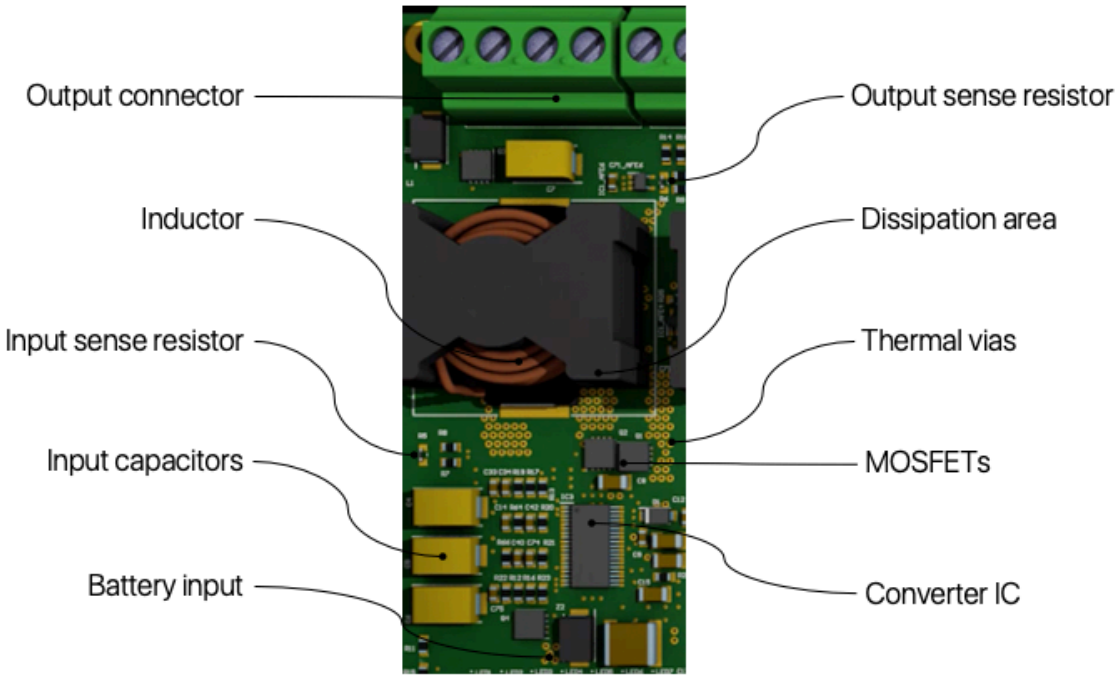


Fig. 4.11: 48 boost converter 3D rendering (PowerModule.PcbDoc)

5. Measurement stage design

The power supply specifications require an accurate measurement of output voltage, output current and power consumption for every channel. To satisfy those requirements, it is necessary to make several design choices.

First of all, a high-side current sensing method is used instead of a low-side sensing. This has the advantage of rejecting the disturbances that could occur on the ground plane, as well as giving the operator the ability to detect load short-circuits [RF10].

Moreover, there are two ways of measuring DC currents: Hall sensing and shunt resistor sensing. Hall sensing measures the magnetic field generated by a wire according to Ampere's law, whereas shunt sensing measures the voltage across a small-value resistor. Although Hall sensing is non-intrusive and does not affect the efficiency of the converter, it is more complex to implement and takes more space on the PCB. A shunt resistor sensing method is therefore preferred. In order to maximise the efficiency of the converter, the current sense resistor required by the converter ICs will be reused. This removes the need for another sense resistor but has the drawback of sensing the inductor current, and not the output current.

After that, a pre-amplifier removes the common-mode component of the differential signal and a filter attenuates high-frequency noise. Finally, an ADC performs the conversion between the analog signal to a digital signal.

The figure below depicts the block diagram of the final design.

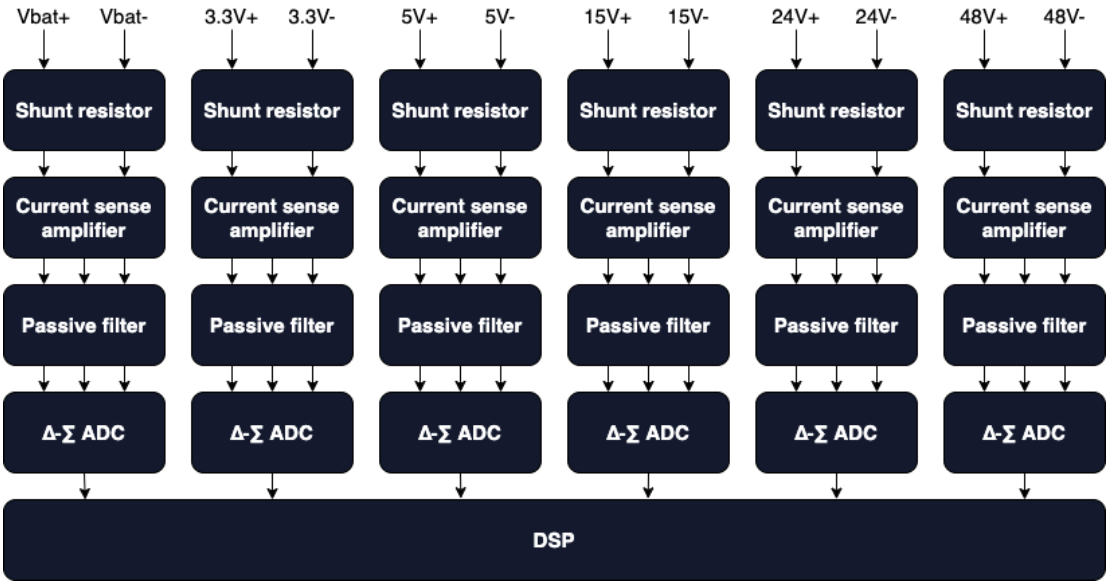


Fig. 5.1: Block diagram of the measurement stage

The high-side current sense is done through a INA290 [RF11] current sense amplifier from Analog Devices. Its common mode rejection must attenuate 60VDC high-side voltage. The implementation of the filter is done using high-quality components (less than 50 ppm/°C). Finally, the analog to digital conversion is performed by multiple STPMS2 [RF12] second-order delta-sigma ADCs from STMicroelectronics. The resulting multiplexed signal is then processed by the DSP in the processing stage.

The top-level diagram representing this concept is shown below.

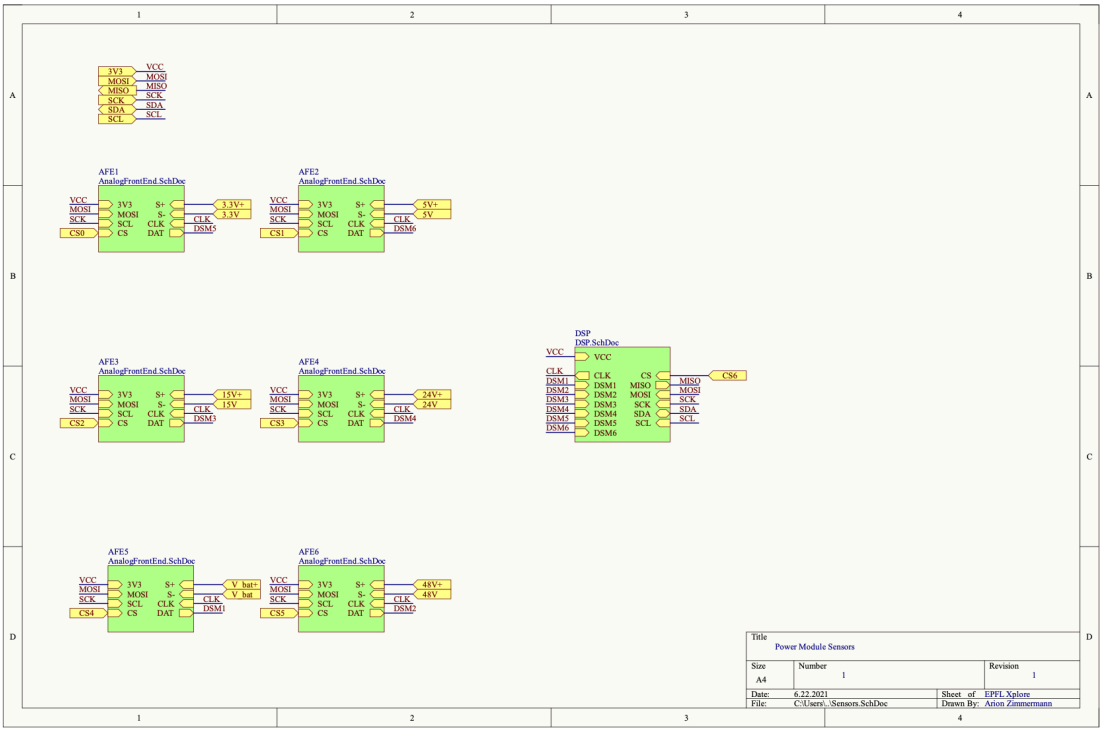


Fig. 5.2: Top-level schematics of the measurement stage (Sensors.SchDoc)

As expected, this schematics consists of 6 Analog-Front-End blocks and 1 DSP block. The Analog-Front-End block can be further expanded in another schematic. The DSP will be further analysed in the next section concerning the processing stage.

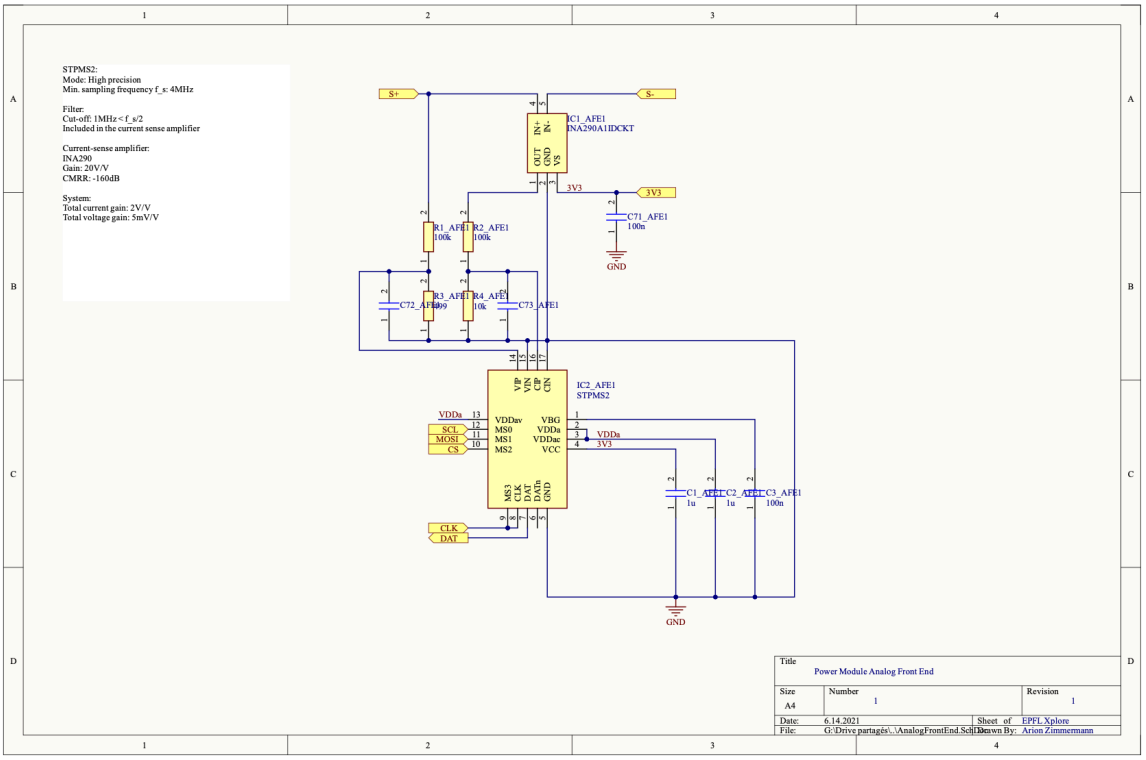


Fig. 5.3: Analog-Front-End Schematic (AnalogFrontEnd.SchDoc)

This analog front end receives two inputs corresponding to the sense resistor terminals S+ and S-. The INA290 amplifies this signal and presents it to the analog filter. A standard cut-off frequency would be of around 10 times the switching frequency of the DC/DC converter. Nevertheless, the exact value of the filter capacitor is left to be determined during testing.

The STPMS2 ADC uses the input current/voltage signals and modulates those into a clocked sigma-delta signal. The advantage of using sigma-delta modulation is that the ADC can multiplex current and voltage measurements on the same line. In fact, the STPMS2 modulates the current measurement when the clock is high and encodes the voltage measurement when the clock is low. Doing so eliminates the phase difference between voltage and current readings and therefore results in a more accurate power calculation.

In addition, this chip can be configured through the SPI protocol, through the sensor bus, as specified in section 3.2.

The six different ADCs are then connected to the DSP described in the next section.

6. Processing stage design

The purpose of the processing stage is to multiply and accumulate the voltage and current measurement, such as to obtain the consumed energy by the Rover. For this, the sigma-delta signals from the analog front ends must be converted through an efficient DSP. The latter must handle and process six signals clocked at 8MHz. Each of those signals consists of multiplexed current and voltage measurements. This means that the current signal is modulated when the clock is high, whereas the voltage signal is encoded when the clock is low. Two delta-sigma demodulators are thus required per output channel.

Indeed, the DSP must embed delta-sigma demodulators that can run in parallel. The perfect candidate for this purpose is the STM32H7A3 [RF13], which has 9 independent Delta-sigma demodulators. Those demodulators have one hardware *sincx* filter each that can increase the valence of the measured signal.

It is clear that 9 demodulators are not enough to handle the 12 delta-sigma signals and a trade-off had to be made. On the one hand, the four channels (Bypass, 15V, 24V, 48V) that have the most energy impact had to be accurately measured. This is why 8 demodulators were dedicated to those. On the other hand, the two systems that have the least energy impact (3.3V, 5V) had to share the same demodulator.

Precise timing is required to measure the energy consumption of the Rover. This is why an external crystal resonator is being used.

Note that a JTAG connection is used to program and debug the microcontroller. External buttons are also used to reset the STM32 and to control the bootloader state.

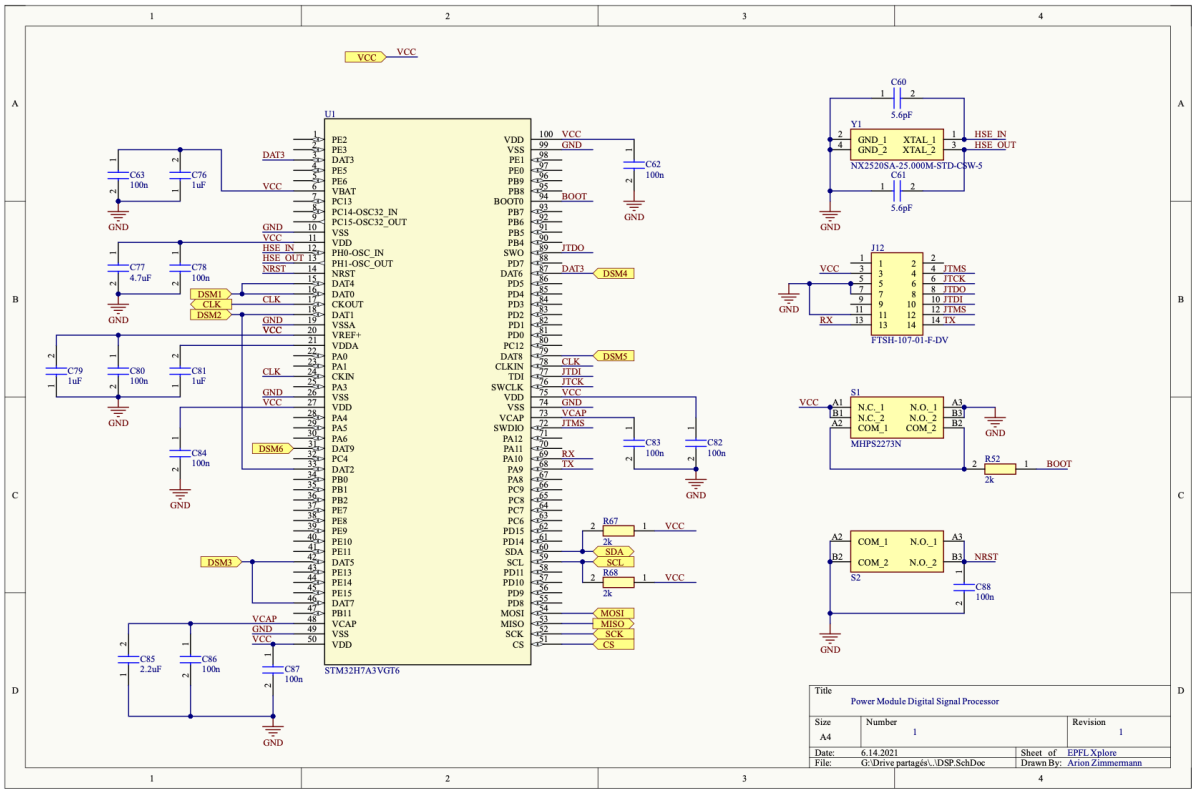


Fig. 6.1: DSP schematic (DSP.SchDoc)

7. Control and telemetry stage design

The power supply's control system is implemented through a dual-core Xtensa 32-bits microprocessor. To facilitate the design, the microprocessor is embedded in a SoC module, which most notably contains Bluetooth and WiFi controllers, and all the I/O features one would expect from a microcontroller. The latter is known as an ESP32-WROOM-UE (ESP32) [RF14] module from Espressif Systems. Using this chip facilitates the integration between the control and the telemetry stages, since both stages can reside on the same hardware.

The control system's purpose is to control the enable pins of the different DC/DC converters and to monitor the voltage, current and power consumption of every output channel. Moreover, the control system must transmit these measurements to remote actors, such as the Rover's Avionics (AV) and the Control Station (CS). Those actors must also be able to enable or disable a given output channel at any moment.

To implement these requirements, the control system implements one high-level interface, accessible by the CS and one low-level interface, accessible by the AV and the CS.

The high-level interface's goal is to provide a basic user interface to the CS' operator, in case the CS hardware fails. This high-level interface must therefore be platform-independent. To do so, it was decided to develop an embedded HTTP server. Using jQuery [RF15] and Bootstrap 3 [RF16], the website allows the teleoperator to monitor and control the power supply remotely.

You may find below an illustration of the power supply's prototype high-level user interface.

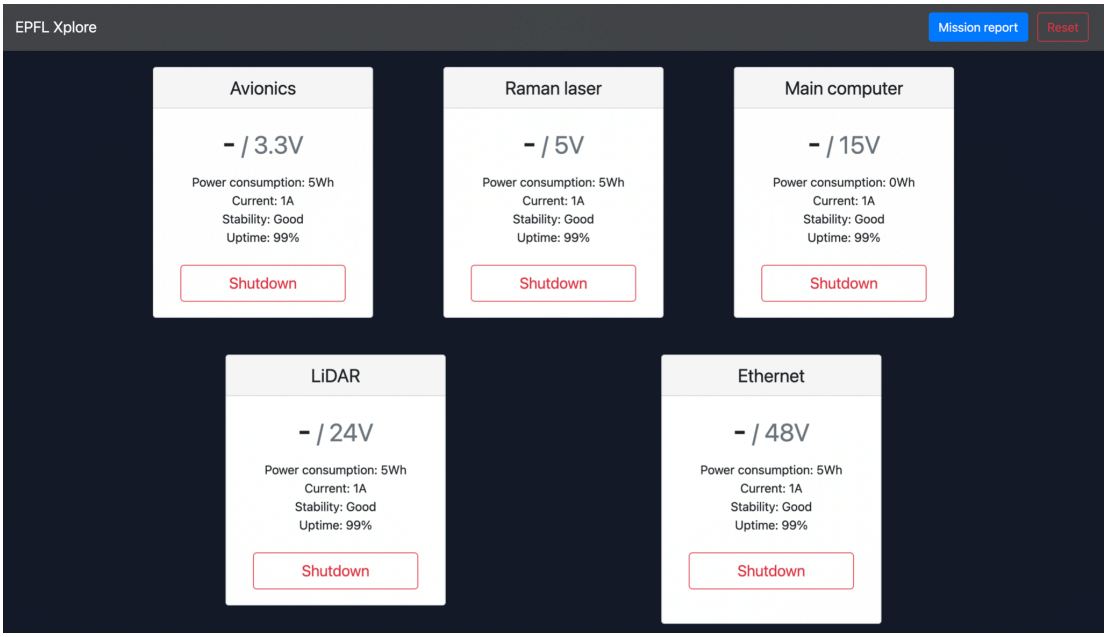


Fig. 7.1: User interface of the power supply

The low-level interface however makes use of RoCo (RoverCommunication), a library I developed in the midst of last year, which provides a modular way of communicating with the rest of the Rover. The power supply is therefore considered as a RoCo node and implements a RoCo TCP/IP driver, as well as a RoCo I^2C driver, to communicate with the CS and the AV respectively.

Thanks to FreeRTOS, a real time operating system, those two interfaces are running in parallel and independently on the ESP32, thereby allowing a fluid user experience.

As a last note, an FTDI chip allows the programming of the ESP32 through a serial port. Note that given the simplicity of the control system, it was deemed unnecessary to develop a JTAG communication with this microcontroller.

Since the ESP32 is a WiFi module, it is necessary to recall the different RF characteristics from the specifications.

RF characteristics

Parameter	Comment	Min.	Typ.	Max.	Unit
Operating frequency	Central frequency (excluding band channels)	-	2.4	-	GHz
RX sensitivity	Independant from antenna gain	-	-100	-90	dBm
TX power	Independant from antenna gain	18	19	-	dBm
TX signal power		-	-	1	W

Table 7.1: RF characteristics

The ESP32 used for the power supply's control system achieves a gain of 19.5dBm, corresponding to 95mW, which fulfills the above TX power requirement. The RX sensitivity is given as -97 dBm at a 1 Mbps modulation.

Moreover, a 2.4GHz IPEX omnidirectional antenna from Molex (2143860001) [RF17], is used. Its peak gain was measured at 5.2dBi and its radiation patterns are shown below. Even though these radiation patterns may look quite non-uniform, this antenna is good enough to test the Rover.

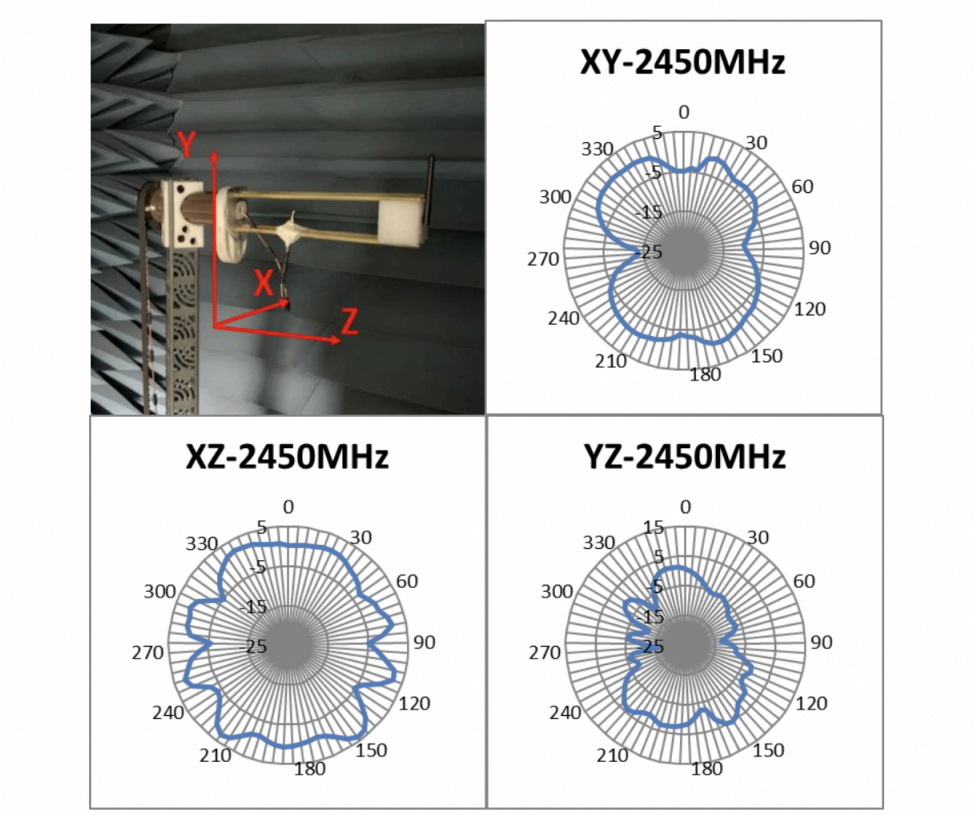


Fig. 7.2: Radiation pattern of the chosen antenna [RF17]

To summarise, a 19.5dBm radio connected to a 5.1dBi antenna can achieve up to 24.6dB system gain. To comply with Swiss regulations that limit 2.4GHz emissions to 100mW EIRP, it is necessary to program the radio such as to limit its emission to 19.5dBm - 4.6dB = 14.9dBm.

8. Final design

This concluding section aims to show the results of the semester project. Since the schematics were already presented in previous sections, this chapter will only show the final PCB layout and rendering, as well as the cost and mass estimate. The remaining schematics are available in Appendix C.

8.1. PCB layout

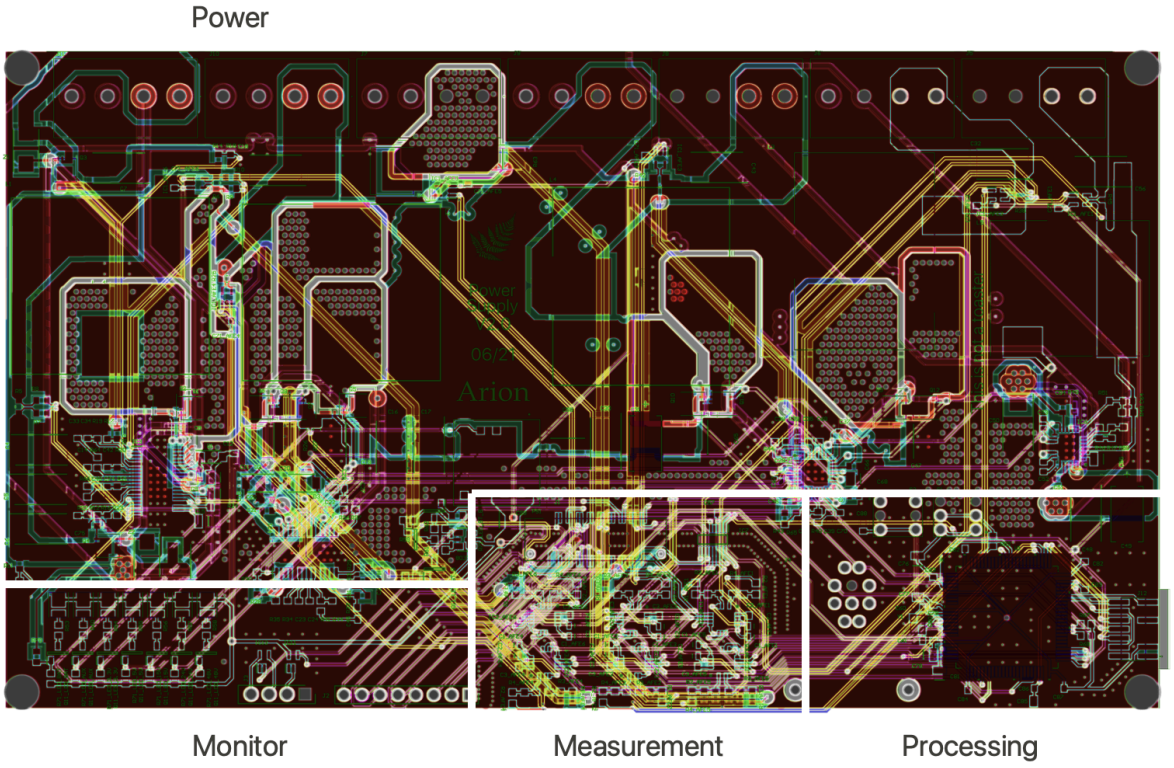


Fig. 8.1: Combined layers of the final PCB design (PowerModule.PcbDoc)

The PCB was divided into four parts. One power stage, one measurement, one processing and one monitor stage. This separation almost complies with the one described at the beginning of the document (section 3.1) with power, measurement and processing stages. The monitor stage simply indicates the state of the output channels. A 40-pins connector resides in the center of this PCB. It is used as an interconnect bus between the power module and the control module. Note that the bold lines on the figure are there to delimitate the different stages but are not physically present on the board.

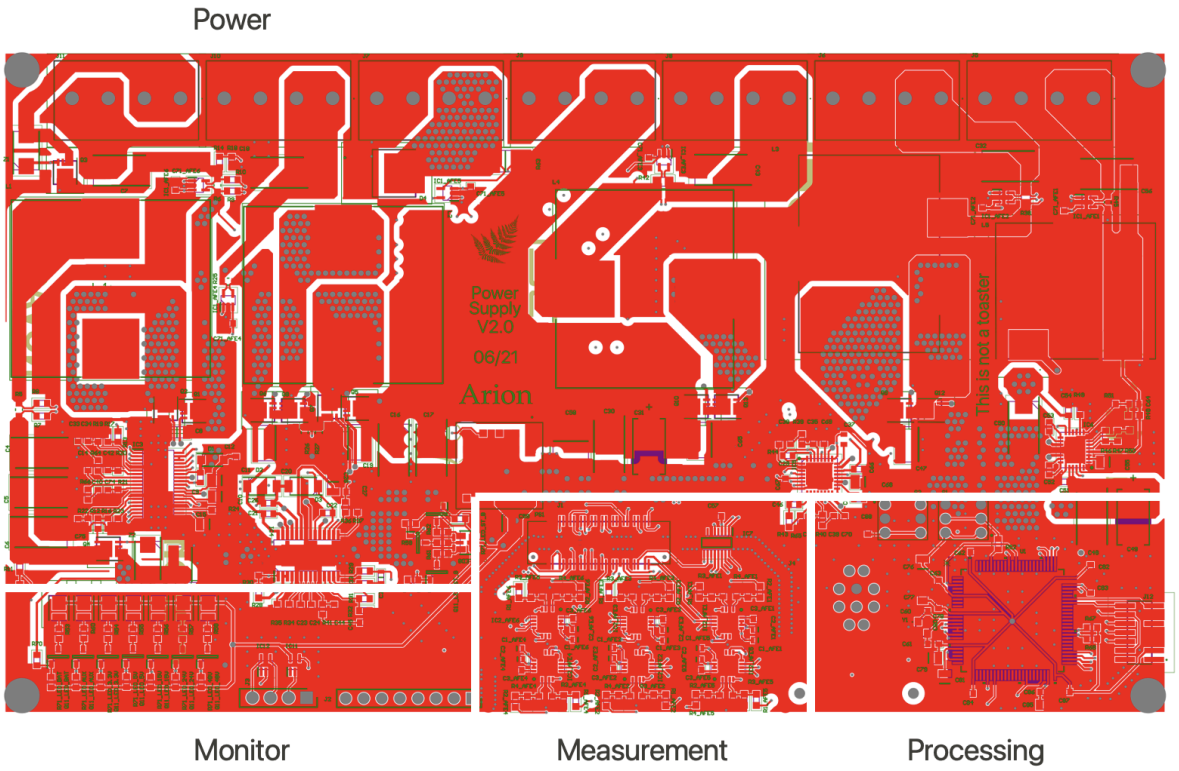


Fig. 8.2: Power layer 1 (PL1) of the final PCB design (PowerModule.PcbDoc)

Large copper polygons are used to transport the power from the input connector to the different output channels.

Cooling areas are omnipresent on the board, as well as thermal vias.

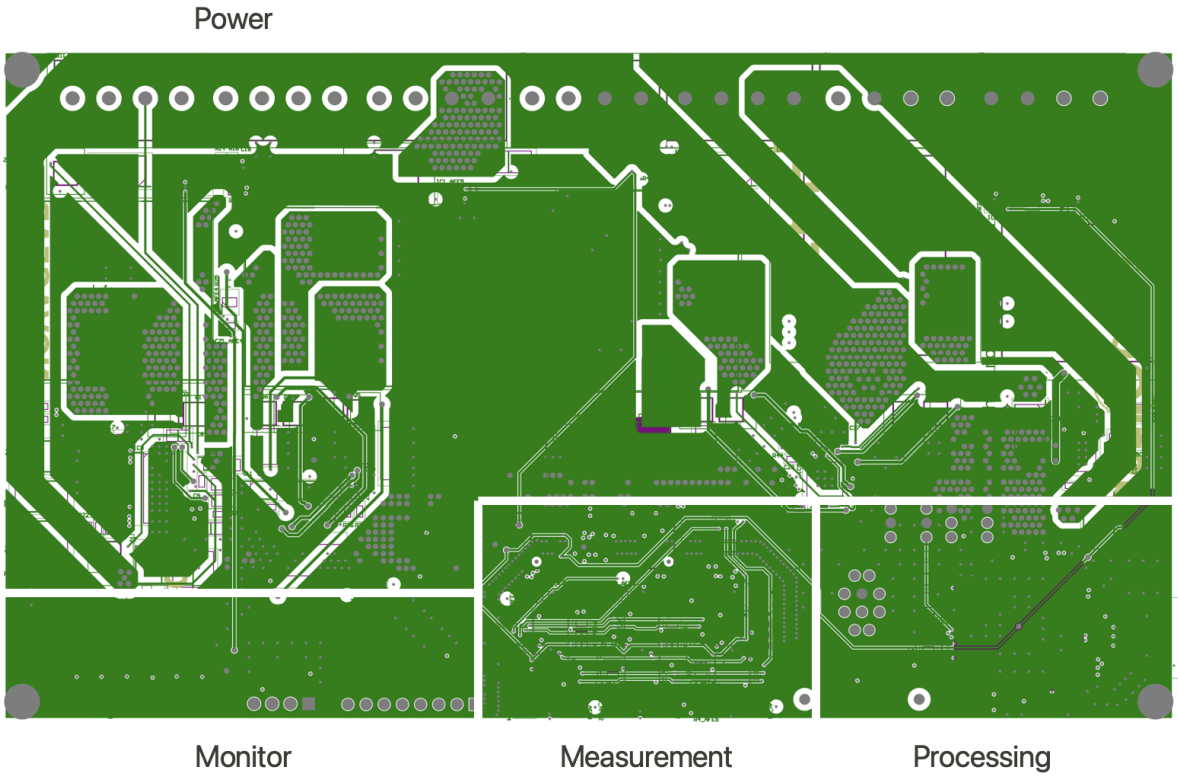


Fig. 8.4: Power layer 1 (PL2) of the final PCB design (PowerModule.PcbDoc)

This layer also transports the battery voltage to the 48V converter and to the 3.3V converter. Several non-sensitive signals also use this layer when necessary. Cooling areas are also present and help dissipate the heat, especially from the MOSFETs.

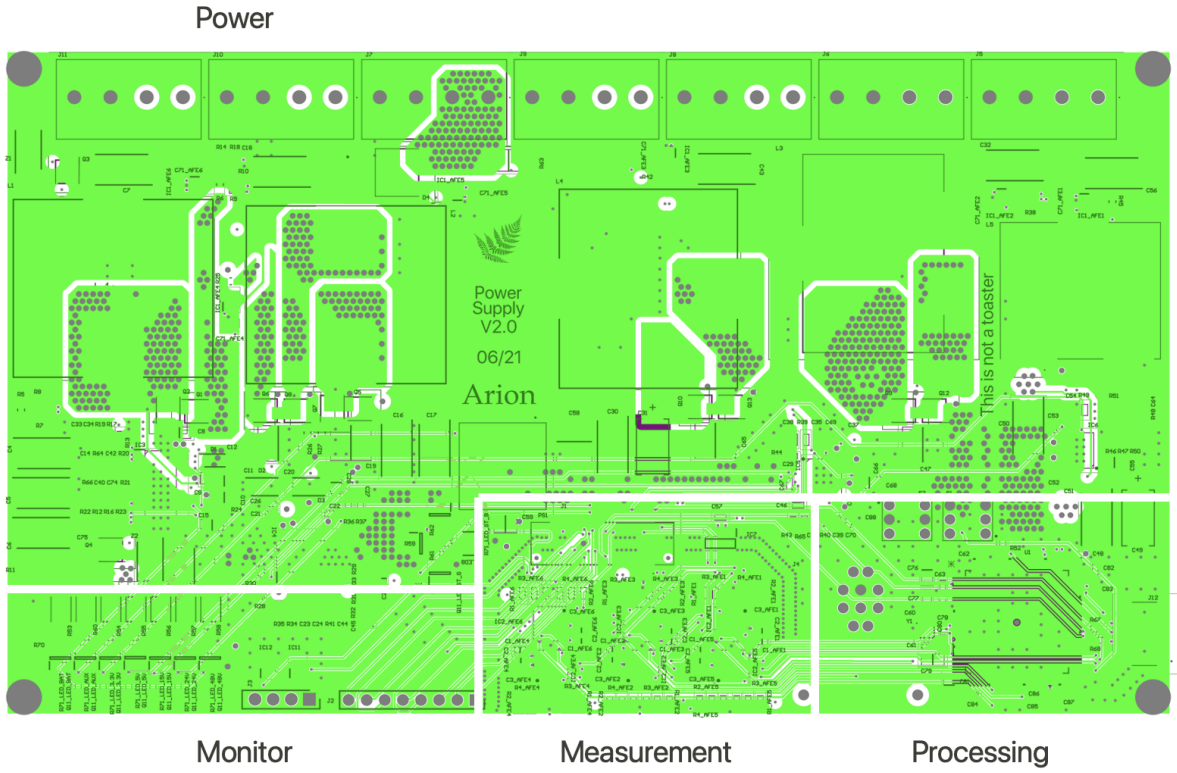


Fig. 8.5: Signal layer 1 (SL1) of the final PCB design (PowerModule.PcbDoc)

This layer mostly consists of miscellaneous horizontal control signals. The multitude of signals on this layer cut the ground plane in many places. The use of vias to connect the cut planes together reduced significantly the inductance of the ground plane.

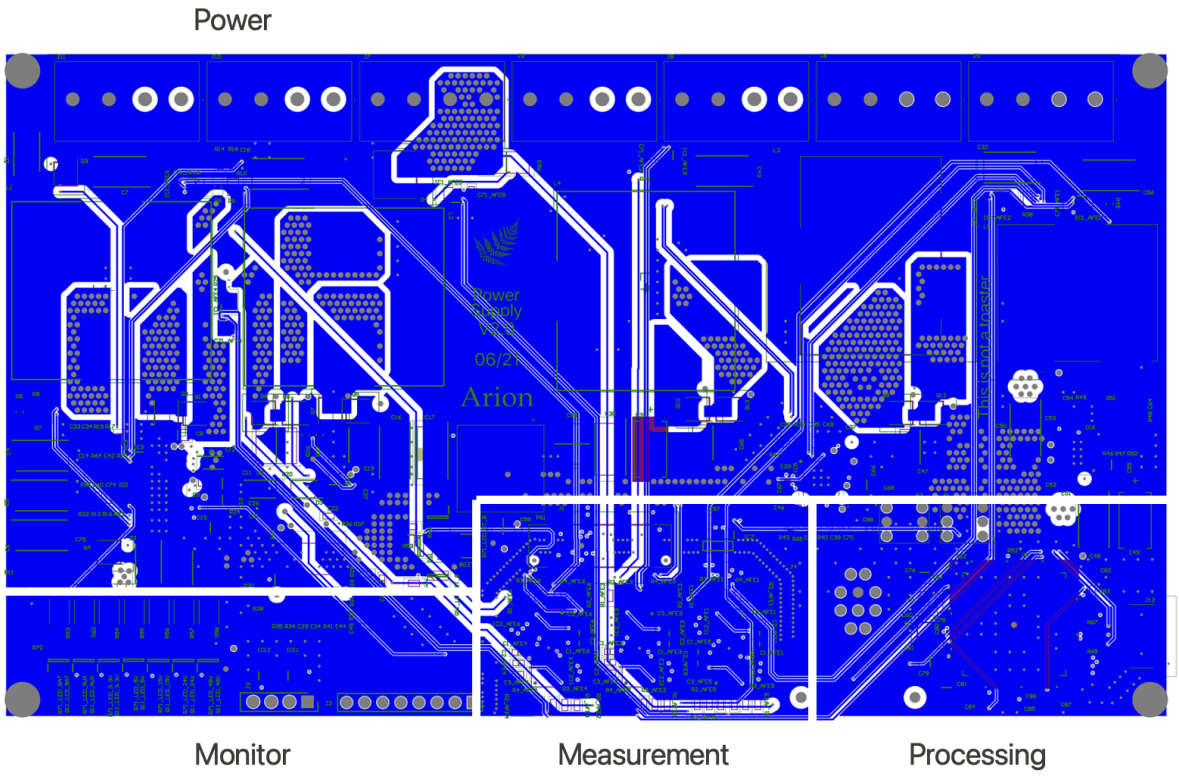


Fig. 8.6: Signal layer 2 (SL2) of the final PCB design (PowerModule.PcbDoc)

This last layer is mainly constituted by analog signals that run vertically through the board. Those signals are used for current sensing and had to be placed as far as possible from the power layer 1 (PL1). It is possible to note that the differential signals are tightly packed together, so that no differential noise is absorbed by the lines.

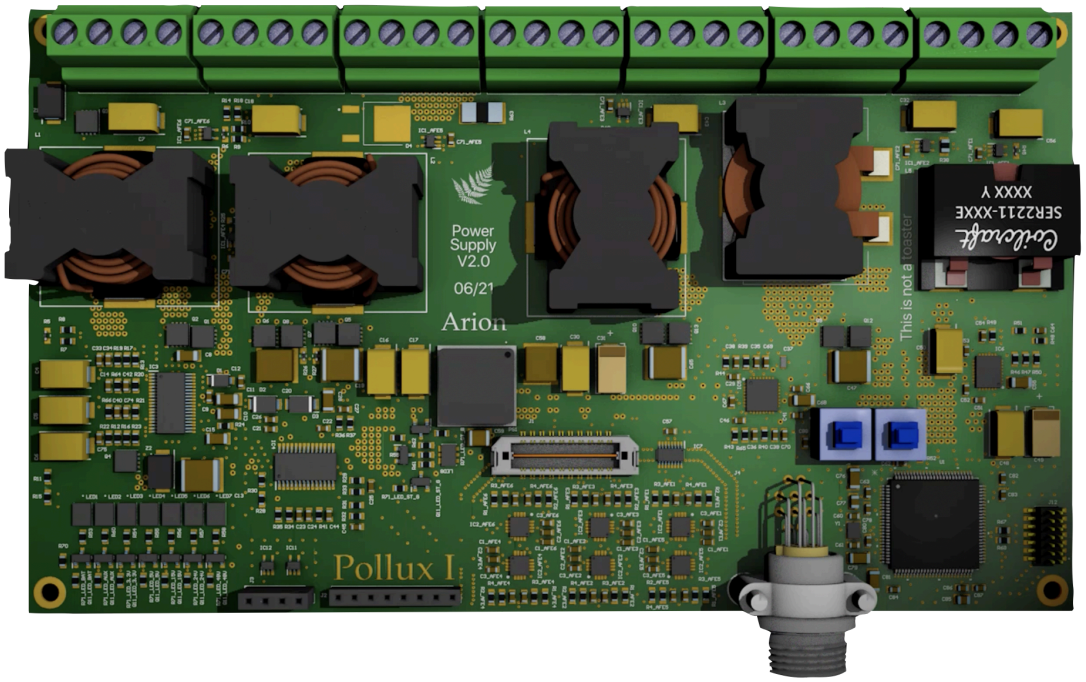


Fig. 6.1: 3D rendering of the final PCB design (PowerModule.PcbDoc)

8.2. Cost estimate

According to the BOM in Appendix B, the different costs related to manufacturing completely one of such a PCB is stated in the table below. A grand total of CHF570 was estimated, of which CHF205 are sponsored. This cost remains in the allocated budget.

Type	Units	Subtotal (CHF)
Ceramic capacitors	104	29.34
Polymer Tantalum e-caps	15	83.25
Connectors	12	124.81
Inductors	5	32.14
Integrated circuits	20	88.80

MOSFETs	22	11.91
Resistors	104	21.04
Others	17	9.4
PCB	3 (min.)	108.87
Stencil	1	27.29
V.A.T		32.92
Total		**569.77**

Table 8.1: Final price estimate

8.3. Mass estimate

Reading the weight of every component on the PCB according to their datasheet yields the following table. The final weight is around 330g, without taking solder into account. This weight is nonetheless clearly smaller than the maximum 400g.

Type	**Units**	**Subtotal (g)**
Ceramic capacitors	104	3.43
Polymer Tantalum e-caps	15	9
Connectors	12	69.07
Inductors	5	151.87
Integrated circuits	20	2.4
MOSFETs	22	2.6
Resistors	104	0.2
Others	17	20
PCB	1	68.73
Total		**327.27**

Table 8.2: Final mass estimate

9. Acknowledgments

Designing a power supply in the scope of this project wouldn't have been possible if it wasn't for all the people who helped and assisted me.

I would like to especially thank my supervisor Jakub Kucka from the Power Electronics Laboratory, who spent many hours reviewing my designs and giving insightful advice.

I would also like to thank Prof. Drazen Dujic from the Power Electronics Laboratory who took this project under the wing of his lab and provided the manufacturing and testing infrastructure which was crucial to this project.

Finally, I would like to acknowledge all my colleagues that helped me design the first power supply prototype, namely Alexandre Devienne (Astrocast), Jérôme Savary (MT-PME), Albéric de Lajarte (MT-PME) and Arno Rogg (NASA).

10. References

ID	Description	Link
[RF01]	Texas Instruments, WEBENCH® Power Designer	https://www.ti.com/design-resources/design-tools-simulation/webench-power-designer.html
[RF02]	Analog Devices, LTC3892 Datasheet and Product Info	https://www.analog.com/en/products/ltc3892.html
[RF03]	Analog Devices, LTC3126 Datasheet and Product Info	https://www.analog.com/en/products/ltc3126.html
[RF04]	Texas Instruments, LM5175 Datasheet and Product Info	https://www.ti.com/product/LM5175
[RF05]	Analog Devices, LT8228 Datasheet and Product Info	https://www.analog.com/en/products/lt8228.html
[RF06]	Infineon, D. Graovac, MOSFET Power Losses Calculation Using the Data- Sheet Parameters	https://application-notes.digchip.com/070/70-41484.pdf
[RF07]	Proprietary, MOSFET losses calculation tool	https://docs.google.com/spreadsheets/d/1Pl5WEU-cmSgak_9eLjTgJyhNc59q_uZr
[RF08]	Infineon, OptiMOS Power-Transistor, 60V, BSZ099N06LS5 datasheet	https://www.infineon.com/dgdl/Infineon-BSZ099N06LS5-DataSheet-v02_04-EN.pdf?fileId=5546d4625696ed760156e5d71c9f4f8e
[RF09]	Texas Instruments, LM5175 Quickstart Calculator	https://www.ti.com/tool/LM5175QUICKSTART-CALC
[RF10]	Texas Instruments, Motaz Khader, System trade-offs for high- and low-side current measurements	https://e2e.ti.com/blogs_/b/analogwire/posts/system-trade-offs-for-high-and-low-side-current-measurements
[RF11]	Texas Instruments, INA290 Datasheet and Product Info	https://www.ti.com/product/INA290
[RF12]	STMicroelectronics, Smart sensor II Dual channel 2nd order sigma-delta modulator with embedded PGA	https://www.st.com/en/data-converters/stpms2.html
[RF13]	STMicroelectronics, STM32H7A3/7B3 product family	https://www.st.com/en/microcontrollers-microprocessors/stm32h7a3-7b3.html
[RF14]	Espressif systems, ESP32-WROOM-32E &	https://www.espressif.com/sites/default/files/documentation/esp32-wroom-32e_esp32-wroom-32u

	ESP32-WROOM-32UE Datasheet	e_datasheet_en.pdf
[RF15]	Opensource, jQuery javascript library	https://jquery.com
[RF16]	Opensource, Bootstrap 3 css library	https://getbootstrap.com/docs/3.3/
[RF17]	Molex, MOLEX WIFI/BT DUAL-BAND ANTENNA I-PEX	https://www.molex.com/pdm_docs/as/2143860001-000.pdf

11. Appendix A: Interconnect pin assignment

Pin ID	Pin Type	Description
1	I/O	Sensor bus signal 0
2	I/O	Sensor bus signal 1
3	I/O	Sensor bus signal 2
4	I/O	Sensor bus signal 3
5	I/O	Sensor bus signal 4
6	I/O	Sensor bus signal 5
7		N.C.
8		N.C.
9	Input	Control bus signal 0
10	Input	Control bus signal 1
11	Input	Control bus signal 2
12	Input	Control bus signal 3
13	Input	Control bus signal 4
14		N.C.
15		N.C.
16		N.C.
17	I/O	System I/O signal 0
18	I/O	System I/O signal 1
19	I/O	System I/O signal 2
20	I/O	System I/O signal 3
21		N.C.
22		N.C.
23	I/O	GPIO 0
24	I/O	GPIO 1

25	I/O	GPIO 2
26	I/O	GPIO 3
27	I/O	GPIO 4
28	I/O	GPIO 5
29	I/O	GPIO 6
30	I/O	GPIO 7
31	Input	Status PWM 1
32	Input	Status PWM 2
33	Input	Status PWM 3
34		N.C.
35	Power	3V3
36	Power	3V3
37	Power	3V3
38	Power	GND
39	Power	GND
40	Power	GND

12. Appendix B: Bill of materials

Item	Type	Reference	Designator(s)	Units	Subtotal
1	Capacitor	80-C0603C104K5R	C3_AFE1, C3_AFE2, C3_AFE3, C3_AFE4, C3_AFE5, C3_AFE6, C9, C12, C14, C21, C22, C25, C26, C29, C33, C34, C40, C42, C45, C46, C51, C52, C53, C54, C57, C62, C63, C66, C67, C69, C70, C71_AFE1, C71_AFE2, C71_AFE3, C71_AFE4, C71_AFE5, C71_AFE6, C72_AFE1, C72_AFE2, C72_AFE3, C72_AFE4, C72_AFE5, C72_AFE6, C73_AFE1, C73_AFE2, C73_AFE3, C73_AFE4, C73_AFE5, C73_AFE6, C74, C75, C78, C80, C82, C83, C84, C86, C87, C88, C89	60	6.3
2	Capacitor	80-C0603C105K8P	C1_AFE1, C1_AFE2, C1_AFE3, C1_AFE4, C1_AFE5, C1_AFE6, C2_AFE1, C2_AFE2, C2_AFE3, C2_AFE4, C2_AFE5, C2_AFE6	12	1.31
3	Capacitor	80-C1206C105M5RECTU	C10, C15, C28, C76, C79, C81	6	1.76
4	Capacitor	581-22201C106KAT2A	C13, C19, C47, C65	4	8.11
5	Capacitor	80-C0603C101M3HACTU	C27, C35, C36, C44	4	0.35584
6	Capacitor	80-C0603C683K5R	C24, C41	2	0.26688
7	Capacitor	80-C1206X475M5RAUTO	C11, C68	2	1.64
8	Capacitor	810-C5750X7R2A475K	C20, C58	2	3.99
9	Capacitor	80-CBR06C569B5GAC	C60, C61	2	0.53376
10	Capacitor	80-C0603C101K5R	C64	1	0.2135
11	Capacitor	80-C0603C102J5R	C39	1	0.08896
12	Capacitor	80-C0603C154K5R	C37	1	0.32915
13	Capacitor	80-C0603C222J5RAUTO	C38	1	0.09786

14	Capacitor	80-C0603C332K5R	C23	1	0.08896
15	Capacitor	80-C0805C225K4RECLR	C85	1	0.26688
16	Capacitor	80-C0805C475J4RAUTO	C77	1	0.51597
17	Capacitor	80-C1206C475K5RAUTO	C55	1	0.96966
18	Capacitor	80-C1210C106K5R	C59	1	1.82
19	Capacitor	810-C3216X8L1H155K16	C8	1	0.68499
20	Capacitor Polarised	80-T523H107M35APE070	C4, C5, C6, C16, C48, C50	6	32.19
21	Capacitor Polarised	80-T521X476M35ATE30	C17, C18, C30, C32, C56	5	37.85
22	Capacitor Polarised	80-T598D336M35E65	C31, C49	2	4.86
23	Capacitor Polarised	80-T521D226M035ATE40	C43	1	3.52
24	Capacitor Polarised	80-T521D475M63ATE075	C7	1	4.83
25	Connector	651-1712805	J5, J6, J7, J8, J9, J10, J11	7	23.79
26	Connector	571-292132-4	J3	1	0.37363
27	Connector	517-929870-01-08-RA	J2	1	1.41
28	Connector	DBPC1031A010-130	J4	1	89.0
29	Connector	200-FTSH10701FDV	J12	1	2.51
30	Connector	200-QTH02001FDDPA	J1	1	7.73
31	Crystal	344-NX2520SA25MSTSW5	Y1	1	0.6583
32	Diode	755-RB088LAM-60TR	D2, D3	2	0.99635
33	Inductor	710-74437529203221	L1, L2	2	16.3
34	Inductor	710-74437529203680	L4	1	8.15
35	Inductor	652-PQ2614BLA-330K	L3	1	3.18
36	Inductor	994-SER2211-473MED	L5	1	4.51
37	Integrated Circuit	595-INA290A1IDCKT	IC1_AFE1, IC1_AFE2, IC1_AFE3, IC1_AFE4, IC1_AFE5, IC1_AFE6	6	17.24
38	Integrated Circuit	511-STPMS2L-PUR	IC2_AFE1, IC2_AFE2, IC2_AFE3, IC2_AFE4, IC2_AFE5, IC2_AFE6	6	12.28
39	Integrated Circuit	595-LM5175PWPR	IC4	1	6.73

40	Integrated Circuit	584-LT8228EFE#PBF	IC3	1	12.41
41	Integrated Circuit	584-LTC3126IUFD#PBF	IC6	1	9.11
42	Integrated Circuit	584-LTC3892EUH-2#PBF	IC5	1	10.52
43	Integrated Circuit	771-NTB0102DP125	IC8	1	0.80954
44	Integrated Circuit	511-STM32H7A3VGT6	U1	1	12.95
45	Integrated Circuit	595-TMUX1308QDYYRQ1	IC7	1	0.4359
46	LED	997-L128BLU10350	LED2	1	0.47149
47	LED	997-L128CYN10350	LED3	1	0.47149
48	LED	997-L128FRD10350	LED7	1	0.665
49	LED	720-KRTBDWLM323A7940	LED8	1	0.843
50	LED	997-L128LME10350	LED4	1	0.63162
51	LED	997-L128MNT10350	LED5	1	0.63162
52	LED	997-L128RNG10350	LED6	1	0.47149
53	LED	997-L128RYL10350	LED1	1	0.48038
54	MOSFET (N-Channel)	726-BSZ099N06LS5ATMA	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q12, Q13	12	8.85
55	MOSFET (N-Channel)	621-DMN2053UW-7	Q11_LED_3.3V, Q11_LED_5V, Q11_LED_15V, Q11_LED_24V, Q11_LED_48V, Q11_LED_AUX, Q11_LED_BAT, Q11_LED_ST_B, Q11_LED_ST_G, Q11_LED_ST_R	10	3.06
56	Power Supply	919-RPMB3.3-3.0	PS1	1	6.31
57	Resistor	71-CRCW060333K0FKEB	R51, R70, R71_LED_3.3V, R71_LED_5V, R71_LED_15V, R71_LED_24V, R71_LED_48V,	12	0.42701

			R71_LED_AUX, R71_LED_BAT, R71_LED_ST_B, R71_LED_ST_G, R71_LED_ST_R		
58	Resistor	594-MCT0603MD1003DP5	R1_AFE1, R1_AFE2, R1_AFE3, R1_AFE4, R1_AFE5, R1_AFE6, R2_AFE1, R2_AFE2, R2_AFE3, R2_AFE4, R2_AFE5, R2_AFE6	12	2.76
59	Resistor	71-CRCW060310K5FKEB	R16, R18, R24, R69, R72, R73, R74, R75	8	0.78285
60	Resistor	71-CRCW0603-21.5K-E3	R20, R22, R52, R64, R66, R67, R68	7	0.68499
61	Resistor	71-CRCW0603J-3-E3	R53, R54, R55, R56, R57, R60	6	0.53376
62	Resistor	71-CRCW0603-249K-E3	R11, R12, R13, R14, R31, R34	6	0.58714
63	Resistor	594-MCT0603MD4990DP5	R3_AFE1, R3_AFE2, R3_AFE3, R3_AFE4, R3_AFE5, R3_AFE6	6	2.08
64	Resistor	594-MCT06030D1002DP5	R4_AFE1, R4_AFE2, R4_AFE3, R4_AFE4, R4_AFE5, R4_AFE6	6	1.65
65	Resistor	71-CRCW0603100KFKEAC	R28, R43, R48, R50	4	0.35584
66	Resistor	71-CRCW0603100RFKEBC	R29, R33, R36, R37	4	0.53376
67	Resistor	71-CRCW060310R0FKEAC	R58, R61, R62	3	0.09786
68	Resistor	71-CRCW0603-1.27K-E3	R9, R10	2	0.19571
69	Resistor	71-CRCW0603-6.49K-E3	R15, R41	2	0.19571
70	Resistor	71-CRCW0603-17.4K	R19, R21	2	0.30246
71	Resistor	71-CRCW0603-787-E3	R7, R8	2	0.19571
72	Resistor	71-WSLP0603R0500FEB	R26, R27	2	2.19
73	Resistor	71-WSLP0603R0600FEB	R6, R45	2	2.15
74	Resistor	71-CRCW06035K62FKEB	R65	1	0.09786
75	Resistor	71-CRCW06037K50FKEB	R39	1	0.09786
76	Resistor	71-CRCW0603-8.66K-E3	R32	1	0.09786
77	Resistor	71-CRCW0603-8.87K-E3	R30	1	0.09786

78	Resistor	71-CRCW060320K0FKEAC	R46	1	0.08896
79	Resistor	71-CRCW060320R0FKEAC	R59	1	0.08896
80	Resistor	71-CRCW0603J-22K-E3	R17	1	0.08896
81	Resistor	71-CRCW0603-24.9K	R44	1	0.15123
82	Resistor	71-CRCW060334K0FKEAC	R40	1	0.10675
83	Resistor	71-CRCW060349K9FKEB	R35	1	0.09786
84	Resistor	71-CRCW060361K9FKEB	R23	1	0.09786
85	Resistor	71-CRCW060380K6FKEB	R47	1	0.09786
86	Resistor	71-CRCW0603-140K-E3	R49	1	0.09786
87	Resistor	652-CSS2H2512R1L00F	R63	1	0.82733
88	Resistor	667-ERJ-6BWFR013V	R42	1	0.64941
89	Resistor	667-ERJ-6LWFR008V	R38	1	0.48038
90	Resistor	71-WSLP0603R0150FEA	R5	1	0.85402
91	Resistor	71-WSLP0603R0250FEA	R25	1	1.2
92	Schottky Diode	511-STPS30170DJF-TR	D4	1	0.99635
93	Schottky Diode	78-V3F6-M3/H	D1	1	0.32026
94	Switch	642-MHPS2273N	S1, S2	2	0.8896
95	Zener Diode	863-1SMB5930BT3G	Z1, Z2	2	0.87181
	Total			**299**	**400.76**

13. Appendix C: Other schematics

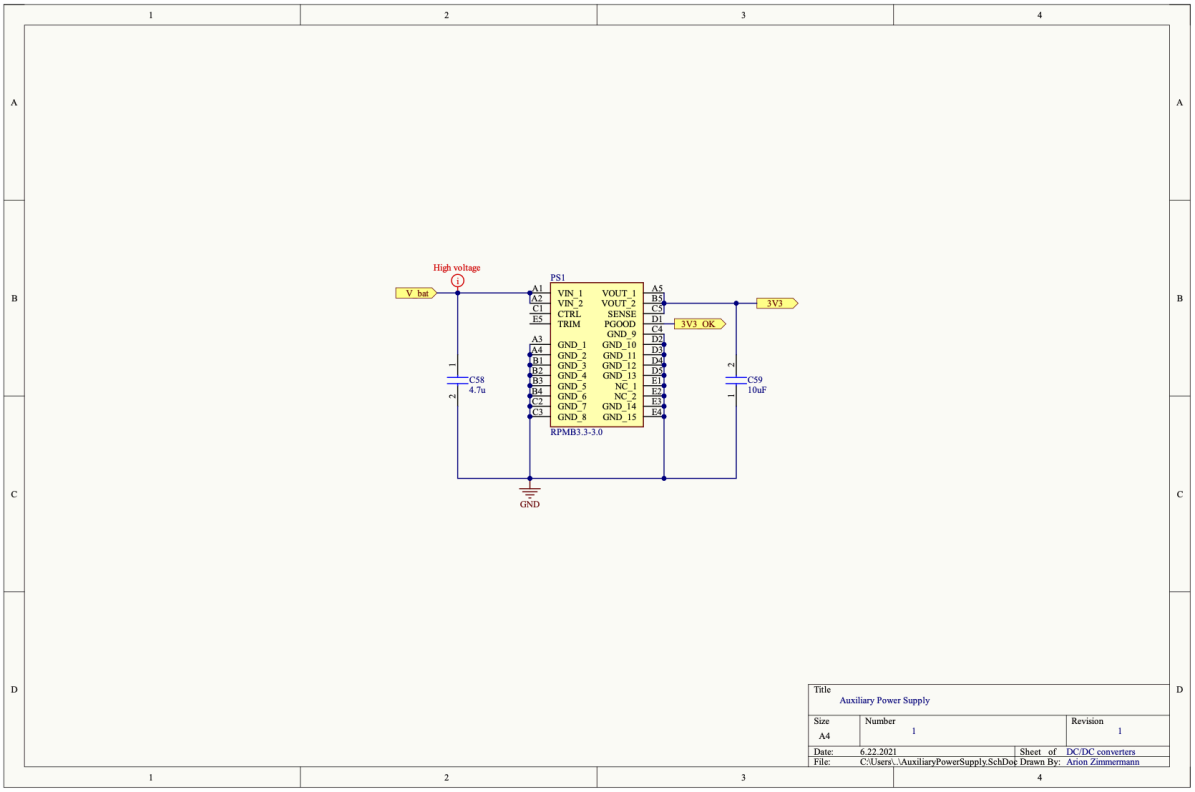


Fig. C.1: Auxiliary power supply schematic (AuxiliaryPowerSupply.SchDoc)

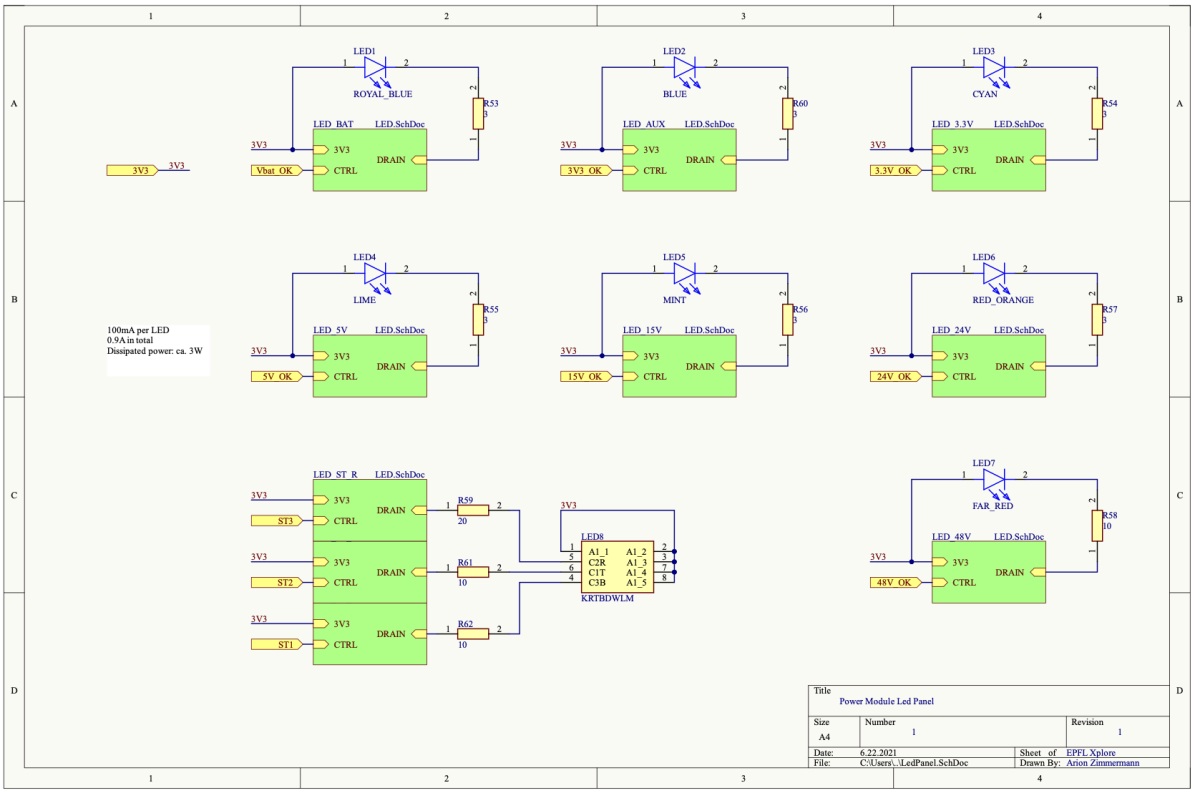


Fig. C.2: LED panel top-level schematic (LedPanel.SchDoc)

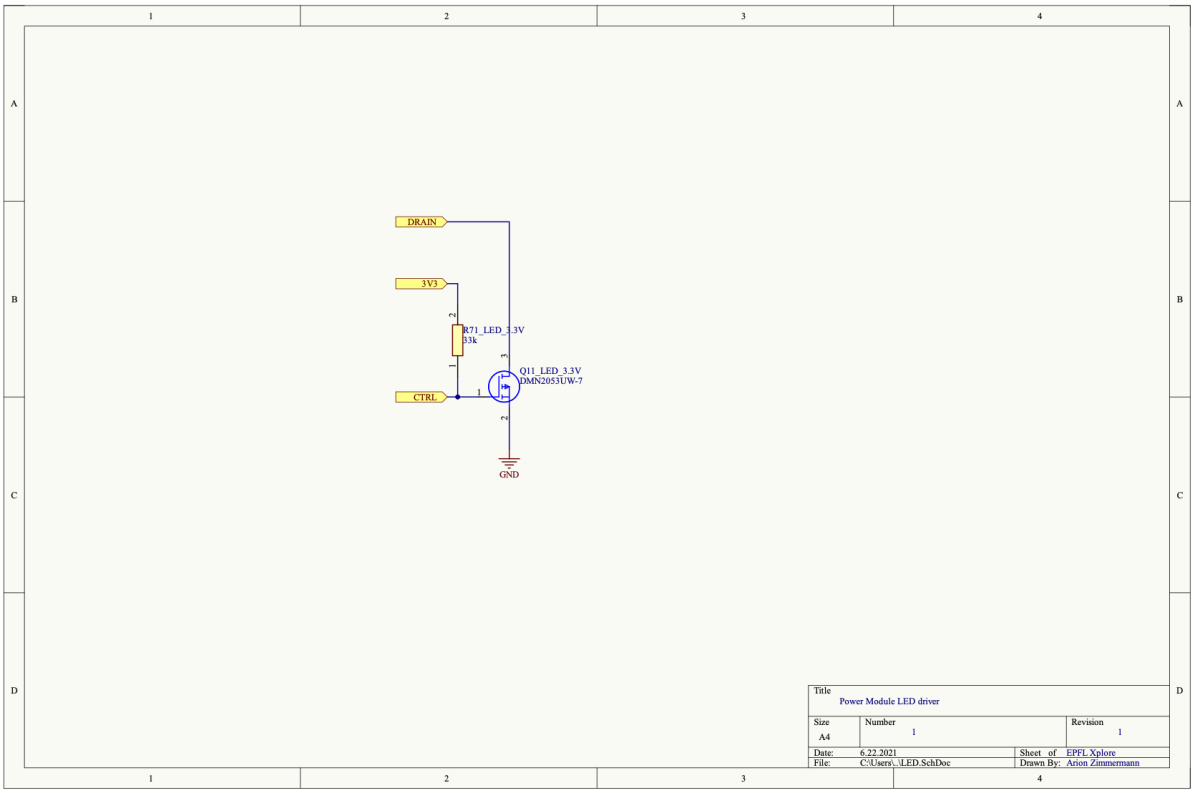


Fig. C.3: LED driver schematic (LED.SchDoc)

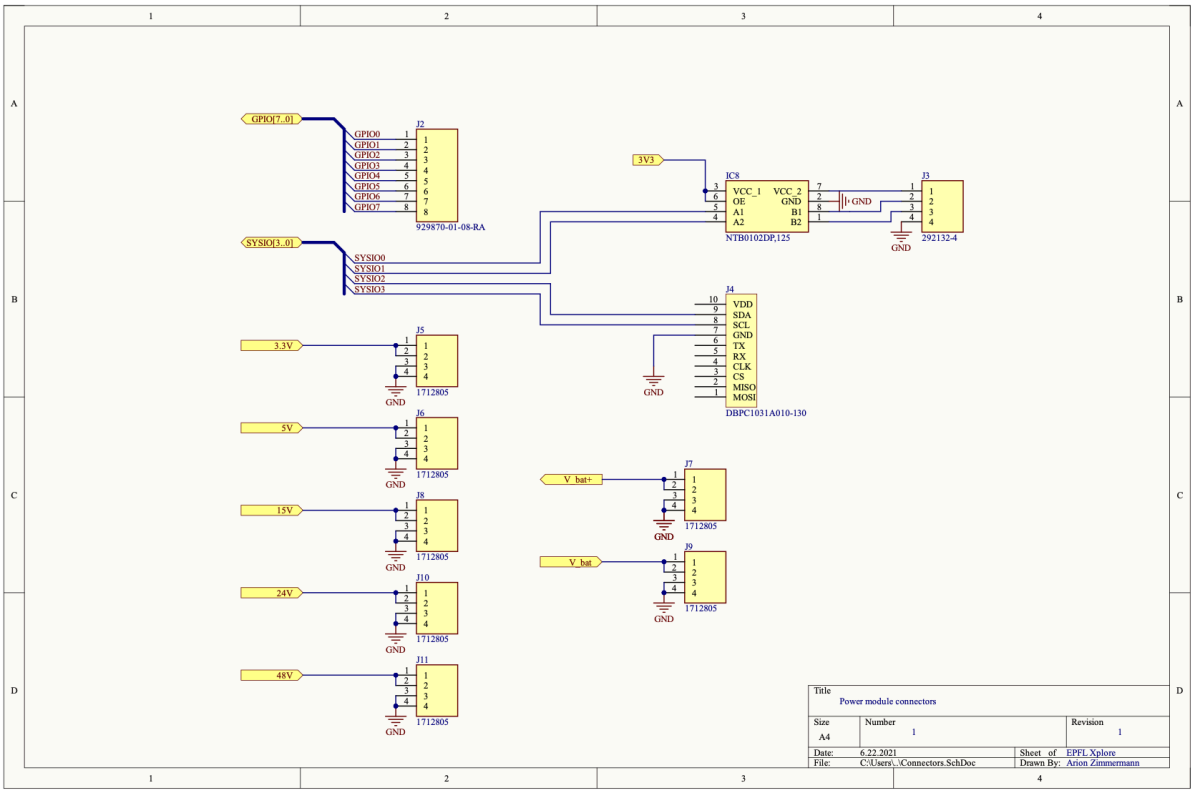


Fig. C.4: Connectors (Connectors.SchDoc)